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05	Clock Diagram	
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09	CPU_DDRIIIB(NEW)	
10	CPU_SATA/SD/PCIE/AZ(NEW)	
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13	CPU_USB/LPC/SMBus(NEW)	
14	CPU_VCC_CORE(NEW)	
15	CPU_POWER(NEW)	
16	CPU_POWER_CAP1(NEW)	
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19	CPU_(STRAP)(NEW)	
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24	VGA(New)	
25	TBD	
26	TBD	
27	USB_HUB(NEW)	
28	USB/USB30(New)	
29	TBD	
30	LAN_RTL8151GD	
31	AUDIO_ALC3600	
32	TBD	
33	TBD	
34	WIRELESS	
35	SATA/LED/BTN	
36	FAN CIRCUITS/HOLE	
37	TBD	
38	SIO_ITE8732(NEW)	
39	DC IN	
40	PWR_3P3V / 5P0V	
41	PWR_12V	
42	1D35V_0D675_TPS51363(NEW)	
43	1P5_S0&1P05_S0&1P8V_S0(NEW)	
44	LDO_CPU_1V_S0&CPU_1V_S5	
45	CPU_CORE&VNN(NEW)	
46	Run_PWR/USB_PWR(NEW)	
47	DSW_POWER_CTL	
48	PWROK(NEW)	
49	GPU(1/5):PCI Express(NEW)	
50	GPU(2/5):_IFB(IO)(NEW)	
51	GPU(3/5):MEMORY_FBA(NEW)	
52	GPU(4/5):GPIO/STRAP(NEW)	
53	GPU(5/5):PWR/GND(NEW)	
54	GPU_DDR3_128MX16(NEW)	
55	GPU_POWER Sequence	
56	GPU_CTF/PPLAY/LDO/MVDD	
57	DC to DC_1D8V_RT8237(NEW)	
58	GPU_VDDC_NCP81172	

BOM Configuration

(R):Unmount

(G):GPU

(U):UMA

(D):Debug used

(C):HDMI Level Shift

(H):HDMI Driver IC

PCB BOARD SIZE

6 Layers

185mm X 244mm

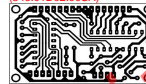
SA BUILD

INTEL Bay Trail Platform

LAN : Gb LAN RTL8151GD

AUDIO: ALC3600

SIO_EC:ITE8732

PCB1
PCB
(348.01D02.00SA)LBL1
LABEL
(45.3E702.001)PCB2
PCB
(348.01D03.00SA)LBL2
LABEL
(40.3EQ13.011)PCB3
PCB
(348.01D04.00SA)

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title Cover Page

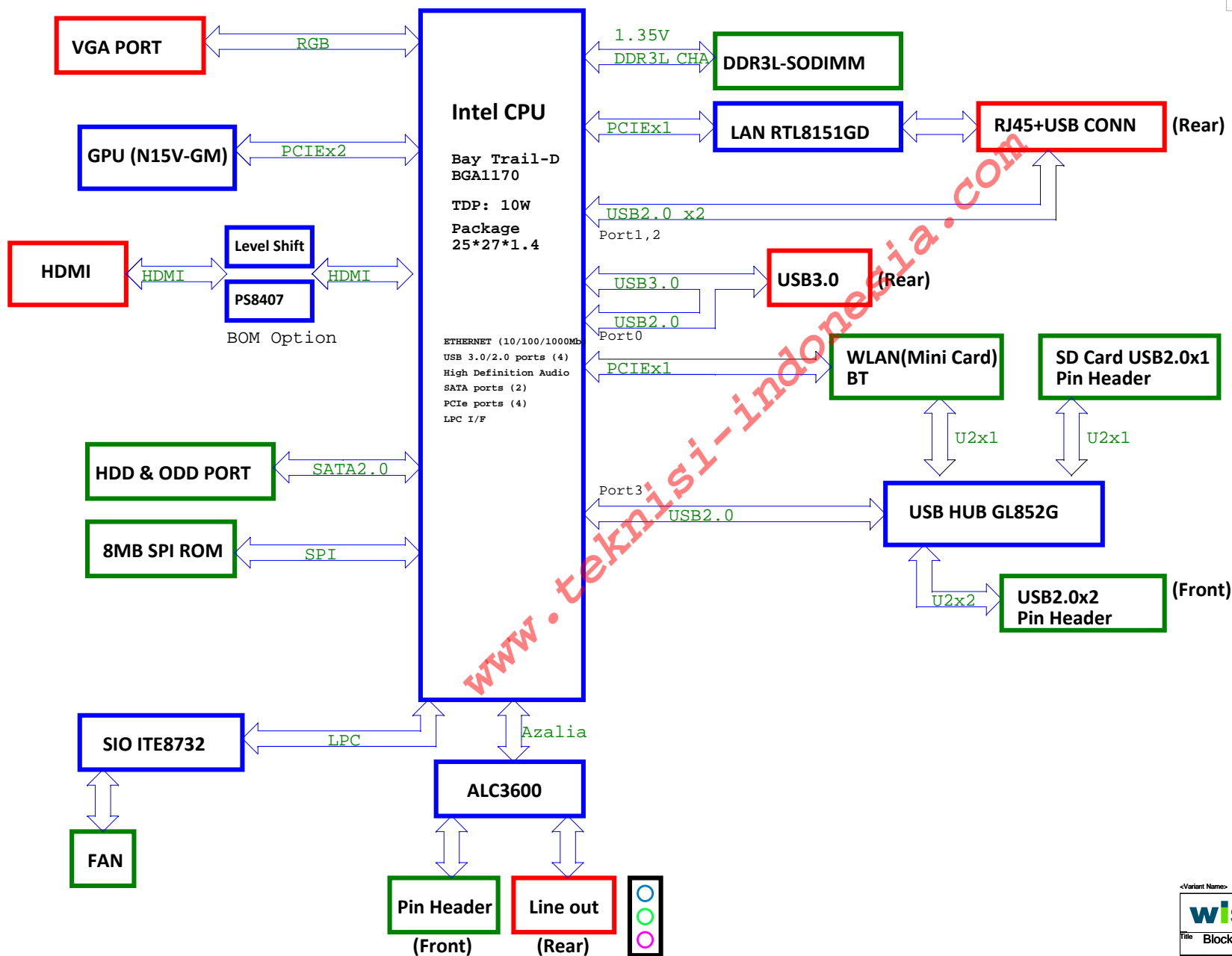
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Rosa_BayTrail_DTRev
A00

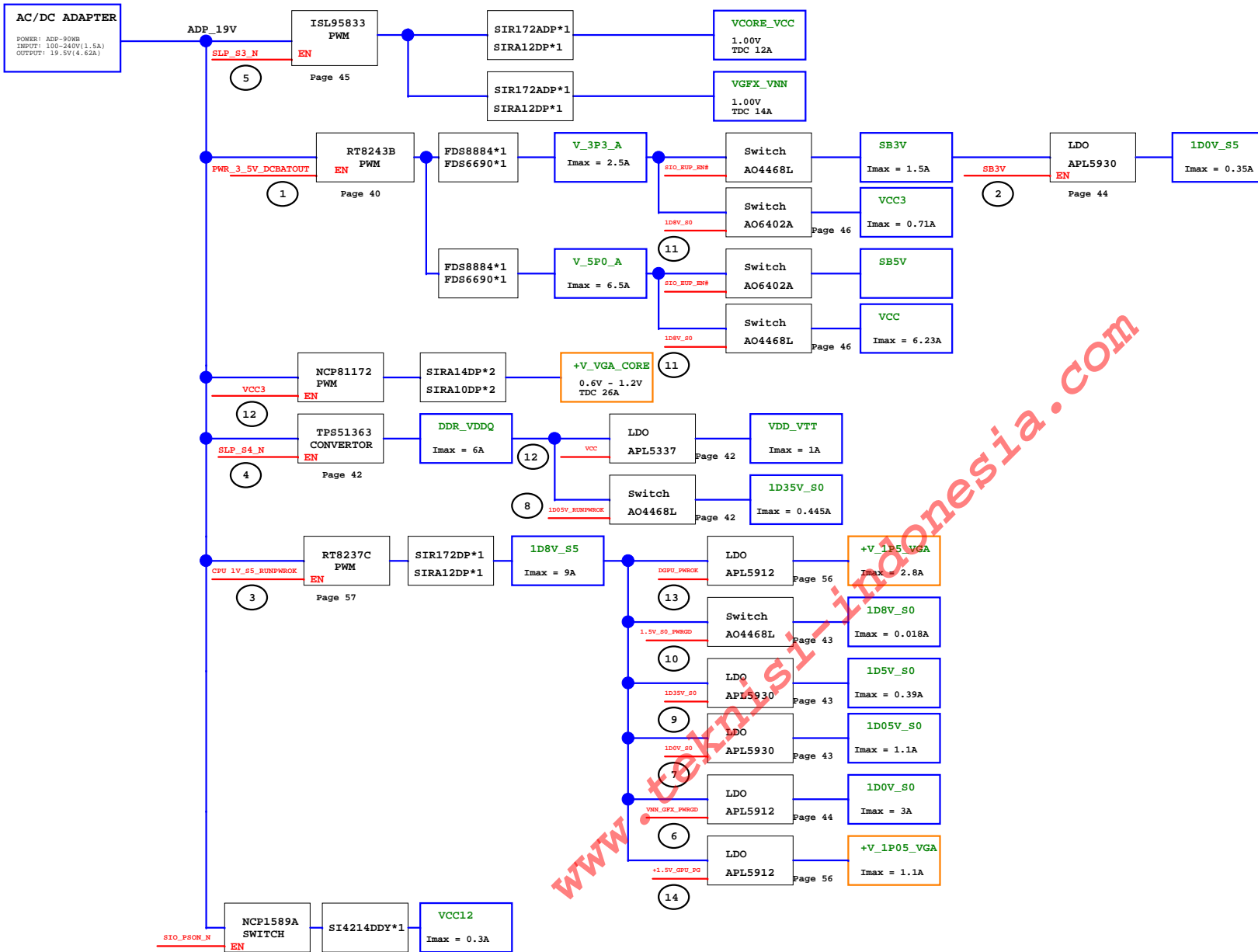
Date: Tuesday, April 15, 2014 Sheet 1 of 58

Project Name: Saffron
Project Code: 3PD01D010001
PCB Version: A00
PCB Number : 14003-1

PCB BOARD SIZE
180mm x 244mm
6 Layer

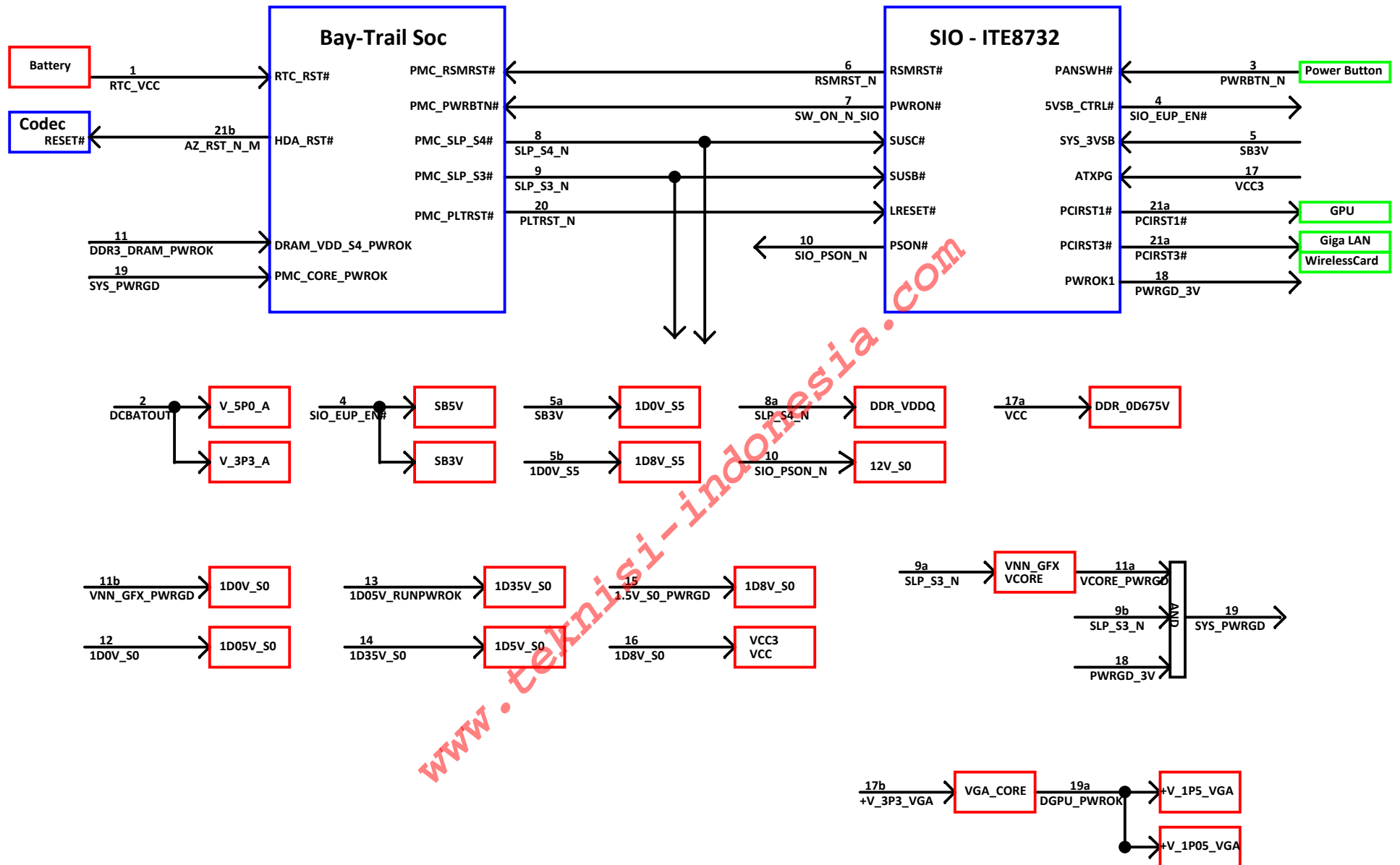
Internal Slot/Header
Front/Rear IO
Chipset

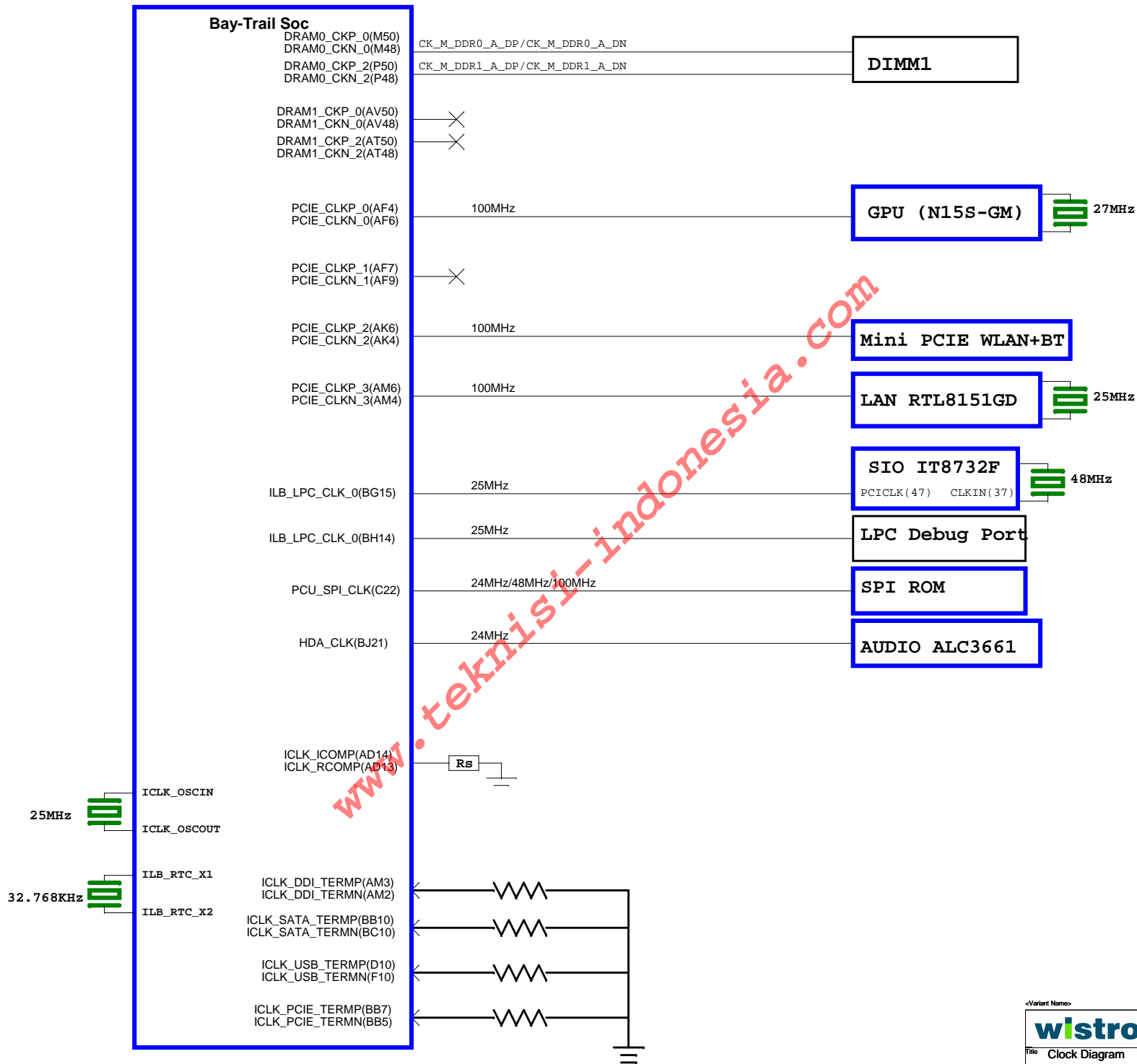




Bay Trail SoC			TDP = 10W
VCORE	VCC	0.40 - 1.14V ; 12A TDC	
VGFX	VNN	0.50 - 1.05V ; 14A TDC	
VDDQ	VDDQ	1.35V ; 1.25A	
1D0V_S5	V1P0A	1.00V ; 0.35A	
1D8V_S5	V1P8A	1.80V ; 0.065A	
V_3P3_A	V3P3A	3.30V ; 0.055A	
1D0V_S0	V1P0S	1.00V ; 3A	
1D05V_S0	V1P05S	1.05V ; 1.1A	
1P35V_S0	V1P35S	1.35V ; 0.445A	
1D8V_S0	V1P8S	1.80V ; 0.018A	
VCC3	V3P3S	3.30V ; 0.03A	
VDD_VTT	VDDQ_VTT	0.675V ; 1A	
V_3P0_BAT_VREG	VRTC	3V ; 100uA (Avg. 6uA)	

SO-DIMM	
DDR_VDDQ	V_MEM_S 1.35V ; 3.75A
VDD_VTT	V_MEM_VTT 0.675V ; 1A
VCC	SIO-IT8732
V_3P3_A	3.3V; 20mA
V_3P3_A	3.3V; 9.37mA
1D8V_S0	BIOS ROM
1D8V_S0	1.8V; 67mA
VCC12	CPU FAN
VCC12	12V; 300mA
VCC5_USB	USB2.0 VBUS
VCC5_USB	5V; 500mA
VCC5_USB	5V; 900mA
V_3P3_LAN	LAN: RTL8151GD
V_1P05_LAN	3.3V; 70mA
V_1P05_LAN	1.05V; 300mA (Internal Switch)
3V_VA	HD CODEC ALC3661-CG
V_5_CODEC	3.3V; 50mA
V_5_CODEC	5V; 50mA
19V_AMP_PVCC	AMP TPAS131
19V_AMP_PVCC	19V; 270mA
DVCC33_2136	DPtoLVDS_RT02136R
DVCC33_2136	3.3V; 180mA
SWR_V12	1.2V; 210mA (Internal Switch)
VCC3	Card Reader RTS5170-GR
VCC3	3.3V; 120mA
V_3P3_PCIVALT	PCI-E Mini Card
V_1P5_PCIE	3.3V; 1.1A
V_1P5_PCIE	1.5V; 0.38A
VCC3_CAM	WEBCAM
VCC3_CAM	3.3V; 240mA
HUB_VCC	USB HUB - GL850-G
HUB_VCC	5V; 52.4mA
V_SHDD	HDD
V_SHDD	5V; 1.1A
V_SHDD	Slim ODD
V_SHDD	5V; 1.5A




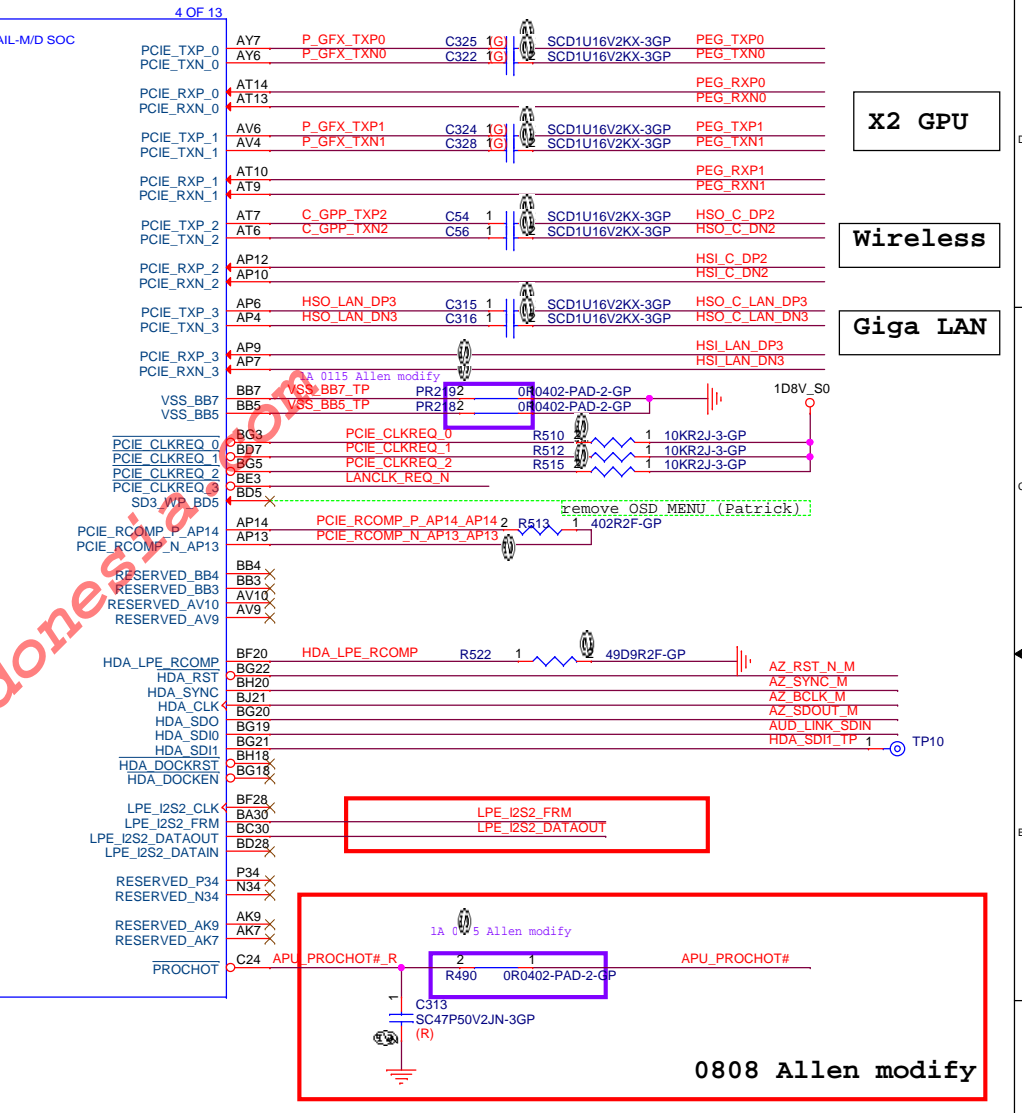
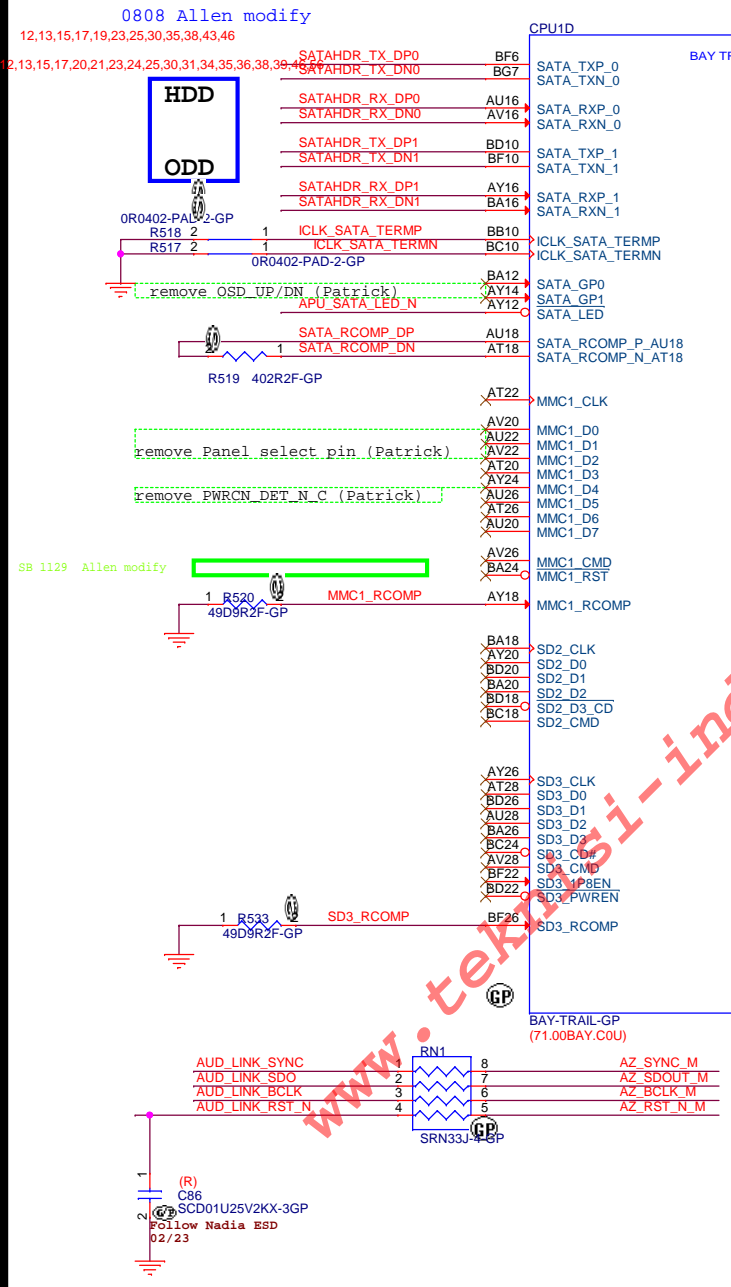
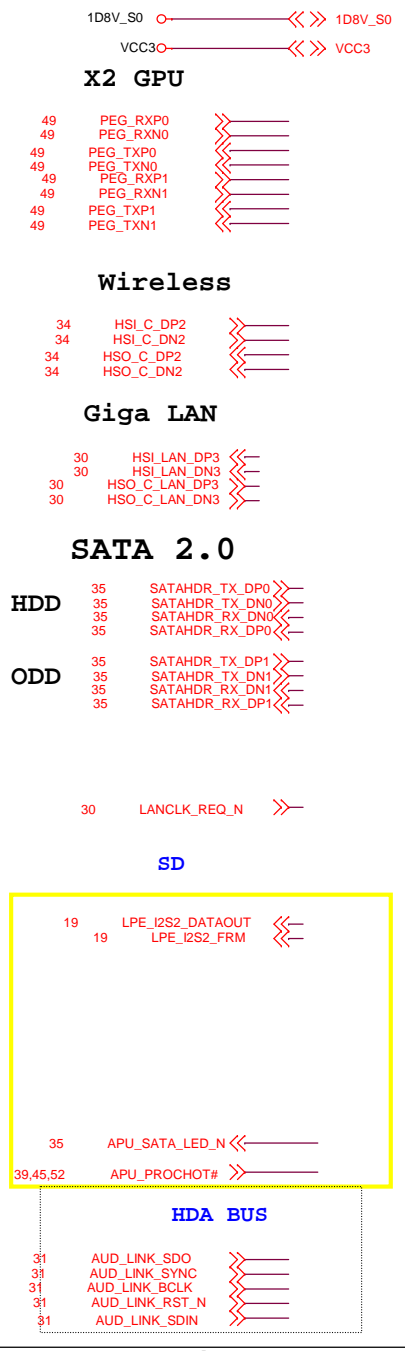


Source Destination Signal



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<Variant Name>		
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TBD		
Size B	Document Number Rosa_BayTrail_DT	Rev A00
Date: Tuesday, April 15, 2014	Sheet 7 of 58	



<Variant Name>

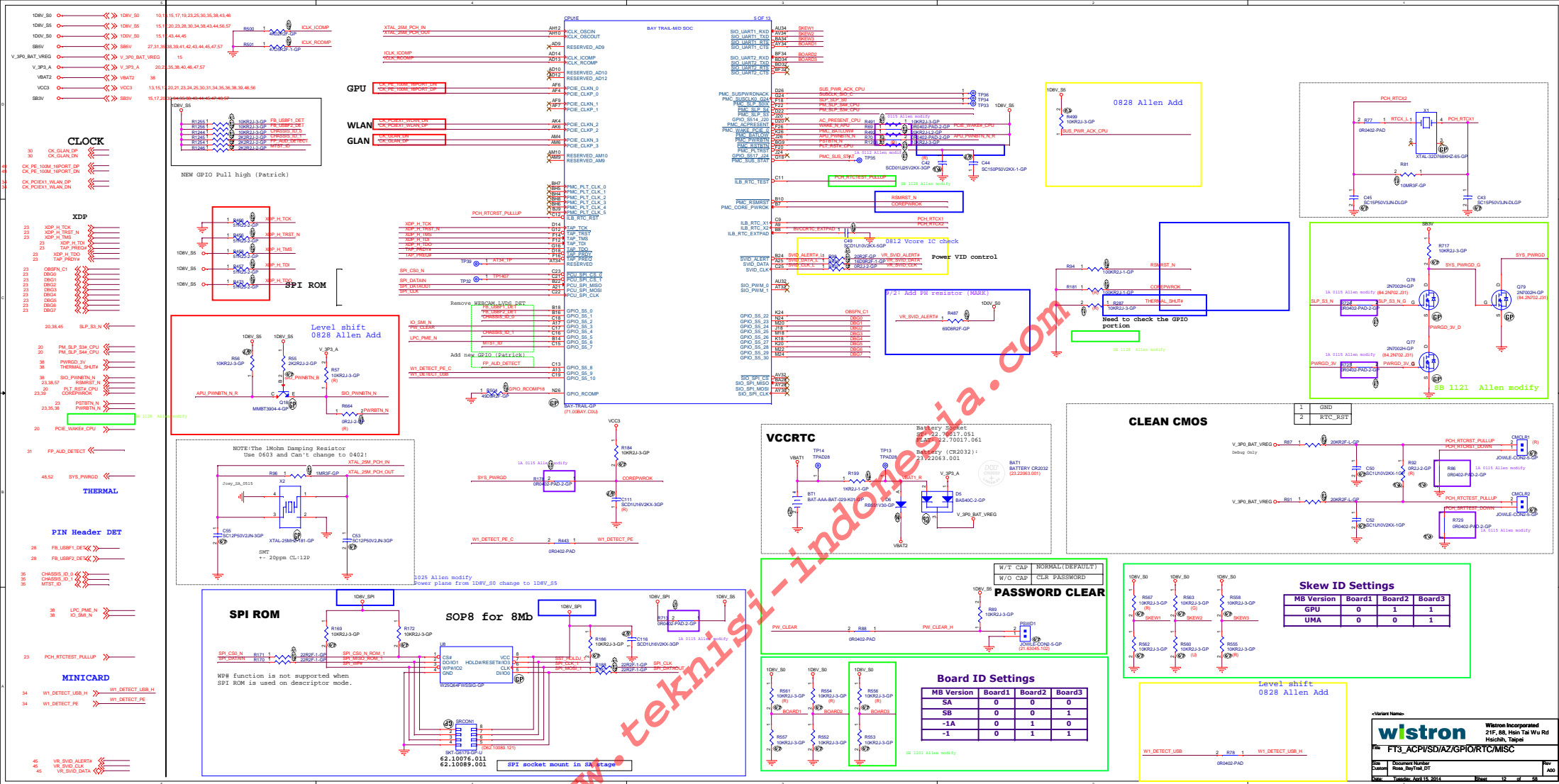
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **09_FT3_PCIE**

Size B	Document Number Rosa_BayTrail_DT	Rev A00
Date: Tuesday, April 15, 2014	Sheet 10	of 58

Size C	Document Number Rosa_BayTrail_DT	Rev A00
Date:	Tuesday, April 15, 2014	Sheet 11 of 58



108V_S0 <<>> 108V_S0 10,12,15,17,19,23,25,30,35,38,43,46
VCC3 <<>> VCC3 12,15,17,20,21,23,24,25,30,31,34,35,36,38,39,46,56

OC <<>>
30 USB0C01 <<>>
28 USB0C02 <<>>

GLAN

12,30 CK_GLAN_DP <<>>
12,30 CK_GLAN_DN <<>>

USB HUB

27 F_USB3P <<>>
27 F_USB3N <<>>

Rear USB

30 F_USB1P <<>>
30 F_USB1N <<>>

30 F_USB2P <<>>
30 F_USB2N <<>>

USB3.0

28 F_USB0P <<>>
28 F_USB0N <<>>

28 USB30_RXP0 <<>>
28 USB30_RXN0 <<>>
28 USB30_TXP0 <<>>
28 USB30_TXN0 <<>>

LPC

23,38 LAD0_FWH0 <<>>
23,38 LAD1_FWH1 <<>>
23,38 LAD2_FWH2 <<>>
23,38 LAD3_FWH3 <<>>
38 INT_SERIRQ_CPU <<>>
23 LPC_CLK1 <<>>
38 CK_25M_SIO <<>>

SMBUS

21,23,38,52 SMB0_CLK <<>>
21,23,38,52 SMB0_DATA <<>>

GPIO

31 APU_SPKR <<>>

19 GPIO_S0_SC_56 <<>>

USB3.0 SIDE I/O

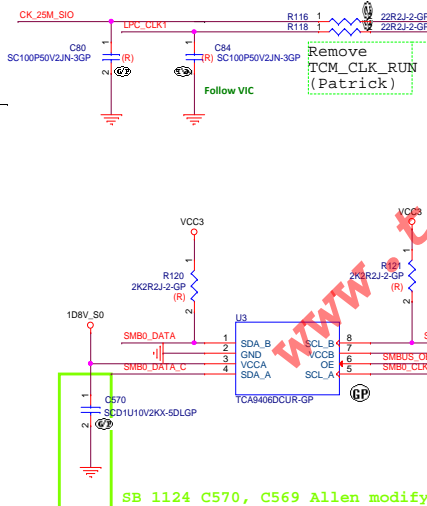
Rear USB

Rear USB

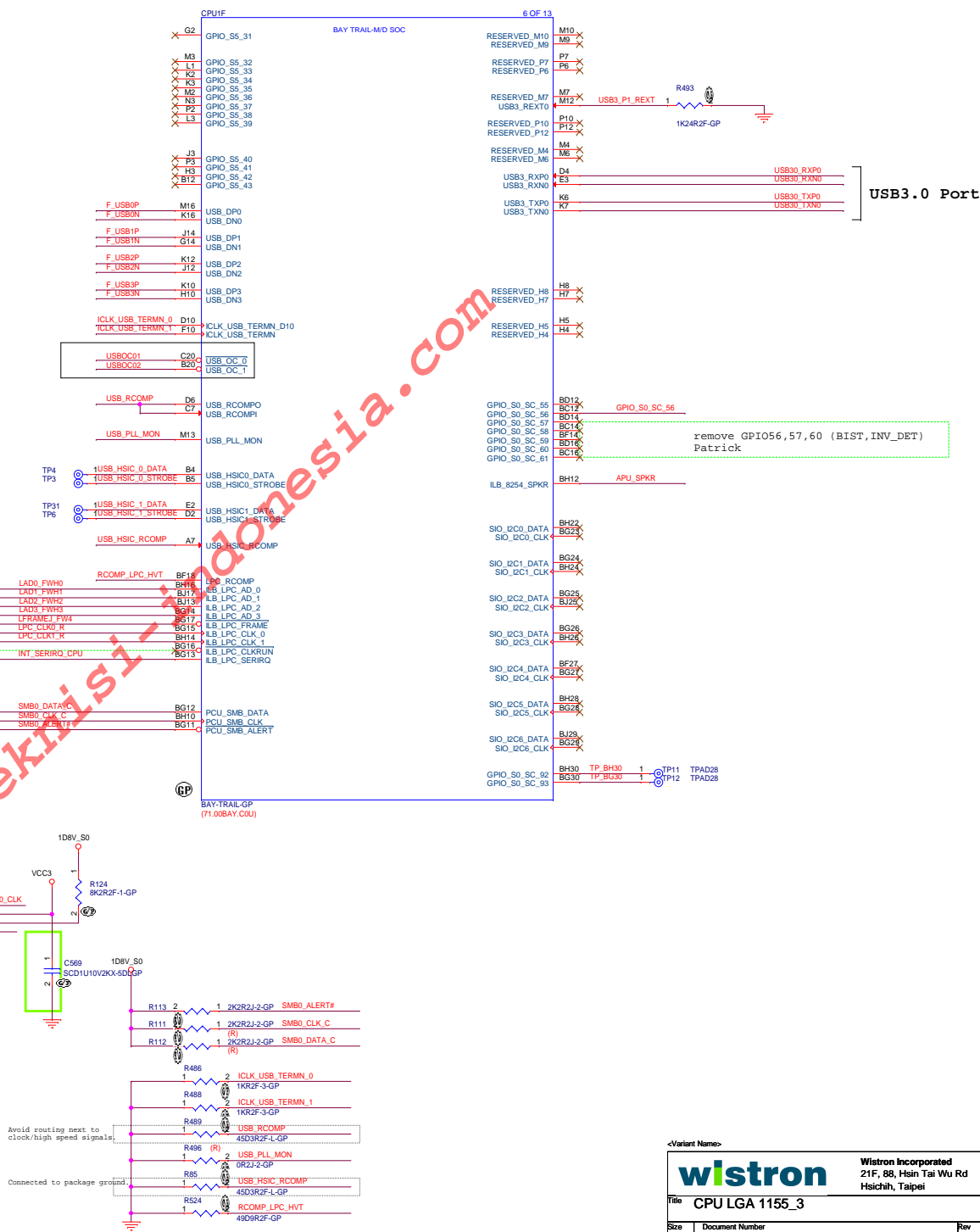
USB HUB

USB0C01 --- Rear IO USB2.0
USB0C02 --- USB3.0

LPC



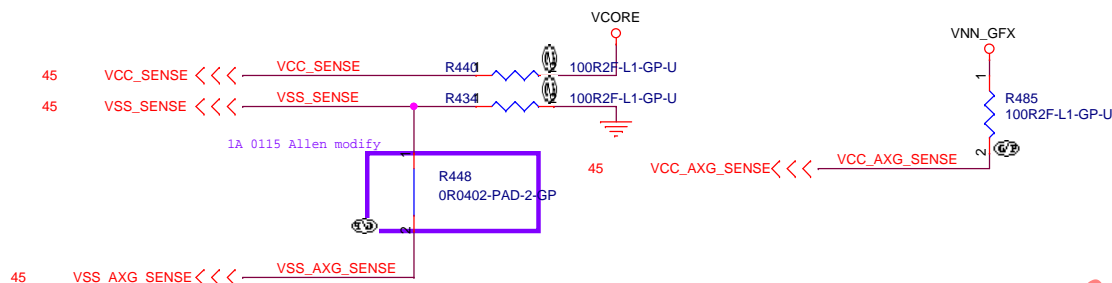
SB 1124 C570, C569 Allen modify



DDR_VDDQ <<>> DDR_VDDQ 8,16,21,42,48
VCORE <<>> VCORE 16,38,45
VNN_GFX <<>> VNN_GFX 16,45

reserve the 0402 0.1u caps on reset for EMI.

VCC_SENSE	C330	(R) 1	SCD1U10V2KX-5GP
VSS_SENSE	C284	(R) 1	SCD1U10V2KX-5GP
VSS_AXG_SENSE	C283	(R) 1	SCD1U10V2KX-5GP
VCC_AXG_SENSE	C312	(R) 1	SCD1U10V2KX-5GP



wistron

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Hsichih, Taipei

Title
CPU (VCC_CORE)

Size
Custom

Date: Tuesday, April 15, 2014

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Rev
A00

1D0V_S0	<<>>	1D0V_S0	12,17,43,44,45
1D05V_S0	<<>>	1D05V_S0	17,43
1D5V_S0	<<>>	1D5V_S0	17,31,34,43
1D8V_S0	<<>>	1D8V_S0	10,12,13,17,19,23,25,30,35,38,43,46
1D8V_S5	<<>>	1D8V_S5	12,17,20,23,28,30,34,38,43,44,56,57
1D35V_S0	<<>>	1D35V_S0	17,42,43
V_3P0_BAT_VREG	<<>>	V_3P0_BAT_VREG	12
V_3P3_A	<<>>	V_3P3_A	12,20,23,35,38,40,46,47,57
VCC3	<<>>	VCC3	12,13,17,20,21,23,24,25,30,31,34,35,36,38,39,46,56
1D0V_S5	<<>>	1D0V_S5	17,44
SB3V	<<>>	SB3V	12,17,20,30,34,35,38,43,44,45,47,48,57

CRB接1.05V

SB 1126 Allen modify

SB 1126 Allen modify

20,42,43

Rogis 20131104
Add power solution for 1D35V_CRT_S0

1D05V_S0 POK
1D05V_RUNPWROK

R730 0R2J-2-GP

PC2123

SCD1U10V2KX-5GP

PC2124

SC10U10V5KX-2GP

PC2125

SC22U6D3V3MX-1-GP

PC2126

SC22U6D3V3MX-1-GP

PC2127

SC22U6D3V3MX-1-GP

PC2128

SC22U6D3V3MX-1-GP

PC2129

SC22U6D3V3MX-1-GP

PC2130

SC22U6D3V3MX-1-GP

PC2131

SC22U6D3V3MX-1-GP

PC2132

SC22U6D3V3MX-1-GP

PC2133

SC22U6D3V3MX-1-GP

PC2134

SC22U6D3V3MX-1-GP

PC2135

SC22U6D3V3MX-1-GP

PC2136

SC22U6D3V3MX-1-GP

PC2137

SC22U6D3V3MX-1-GP

PC2138

SC22U6D3V3MX-1-GP

PC2139

SC22U6D3V3MX-1-GP

PC2140

SC22U6D3V3MX-1-GP

PC2141

SC22U6D3V3MX-1-GP

PC2142

SC22U6D3V3MX-1-GP

PC2143

SC22U6D3V3MX-1-GP

PC2144

SC22U6D3V3MX-1-GP

PC2145

SC22U6D3V3MX-1-GP

PC2146

SC22U6D3V3MX-1-GP

PC2147

SC22U6D3V3MX-1-GP

PC2148

SC22U6D3V3MX-1-GP

PC2149

SC22U6D3V3MX-1-GP

PC2150

SC22U6D3V3MX-1-GP

PC2151

SC22U6D3V3MX-1-GP

PC2152

SC22U6D3V3MX-1-GP

PC2153

SC22U6D3V3MX-1-GP

PC2154

SC22U6D3V3MX-1-GP

PC2155

SC22U6D3V3MX-1-GP

PC2156

SC22U6D3V3MX-1-GP

PC2157

SC22U6D3V3MX-1-GP

PC2158

SC22U6D3V3MX-1-GP

PC2159

SC22U6D3V3MX-1-GP

PC2160

SC22U6D3V3MX-1-GP

PC2161

SC22U6D3V3MX-1-GP

PC2162

SC22U6D3V3MX-1-GP

PC2163

SC22U6D3V3MX-1-GP

PC2164

SC22U6D3V3MX-1-GP

PC2165

SC22U6D3V3MX-1-GP

PC2166

SC22U6D3V3MX-1-GP

PC2167

SC22U6D3V3MX-1-GP

PC2168

SC22U6D3V3MX-1-GP

PC2169

SC22U6D3V3MX-1-GP

PC2170

SC22U6D3V3MX-1-GP

PC2171

SC22U6D3V3MX-1-GP

PC2172

SC22U6D3V3MX-1-GP

PC2173

SC22U6D3V3MX-1-GP

PC2174

SC22U6D3V3MX-1-GP

PC2175

SC22U6D3V3MX-1-GP

PC2176

SC22U6D3V3MX-1-GP

PC2177

SC22U6D3V3MX-1-GP

PC2178

SC22U6D3V3MX-1-GP

PC2179

SC22U6D3V3MX-1-GP

PC2180

SC22U6D3V3MX-1-GP

PC2181

SC22U6D3V3MX-1-GP

PC2182

SC22U6D3V3MX-1-GP

PC2183

SC22U6D3V3MX-1-GP

PC2184

SC22U6D3V3MX-1-GP

PC2185

SC22U6D3V3MX-1-GP

PC2186

SC22U6D3V3MX-1-GP

PC2187

SC22U6D3V3MX-1-GP

PC2188

SC22U6D3V3MX-1-GP

PC2189

SC22U6D3V3MX-1-GP

PC2190

SC22U6D3V3MX-1-GP

PC2191

SC22U6D3V3MX-1-GP

PC2192

SC22U6D3V3MX-1-GP

PC2193

SC22U6D3V3MX-1-GP

PC2194

SC22U6D3V3MX-1-GP

PC2195

SC22U6D3V3MX-1-GP

PC2196

SC22U6D3V3MX-1-GP

PC2197

SC22U6D3V3MX-1-GP

PC2198

SC22U6D3V3MX-1-GP

PC2199

SC22U6D3V3MX-1-GP

PC2200

SC22U6D3V3MX-1-GP

PC2201

SC22U6D3V3MX-1-GP

PC2202

SC22U6D3V3MX-1-GP

PC2203

SC22U6D3V3MX-1-GP

PC2204

SC22U6D3V3MX-1-GP

PC2205

SC22U6D3V3MX-1-GP

PC2206

SC22U6D3V3MX-1-GP

PC2207

SC22U6D3V3MX-1-GP

PC2208

SC22U6D3V3MX-1-GP

PC2209

SC22U6D3V3MX-1-GP

PC2210

SC22U6D3V3MX-1-GP

PC2211

SC22U6D3V3MX-1-GP

PC2212

SC22U6D3V3MX-1-GP

PC2213

SC22U6D3V3MX-1-GP

PC2214

SC22U6D3V3MX-1-GP

PC2215

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PC2216

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PC2217

SC22U6D3V3MX-1-GP

PC2218

SC22U6D3V3MX-1-GP

PC2219

SC22U6D3V3MX-1-GP

PC2220

SC22U6D3V3MX-1-GP

PC2221

SC22U6D3V3MX-1-GP

PC2222

SC22U6D3V3MX-1-GP

PC2223

SC22U6D3V3MX-1-GP

PC2224

SC22U6D3V3MX-1-GP

PC2225

SC22U6D3V3MX-1-GP

PC2226

SC22U6D3V3MX-1-GP

PC2227

SC22U6D3V3MX-1-GP

PC2228

SC22U6D3V3MX-1-GP

PC2229

SC22U6D3V3MX-1-GP

PC2230

SC22U6D3V3MX-1-GP

PC2231

SC22U6D3V3MX-1-GP

PC2232

SC22U6D3V3MX-1-GP

PC2233

SC22U6D3V3MX-1-GP

PC2234

SC22U6D3V3MX-1-GP

PC2235

SC22U6D3V3MX-1-GP

PC2236

SC22U6D3V3MX-1-GP

PC2237

SC22U6D3V3MX-1-GP

PC2238

SC22U6D3V3MX-1-GP

PC2239

SC22U6D3V3MX-1-GP

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SC22U6D3V3MX-1-GP

PC2242

SC22U6D3V3MX-1-GP

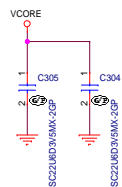
PC2243

SC22U6D3V3MX-1-GP

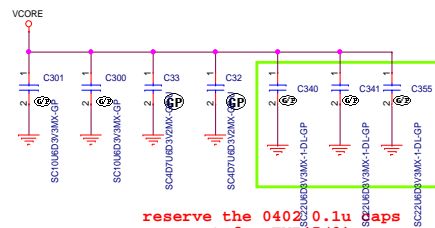
PC2244

VCORE <<< VCORE 14,38,45
 VNN_GFX <<< VNN_GFX 14,45
 DDR_VDDQ <<< DDR_VDDQ 8,14,21,42,48

VCORE

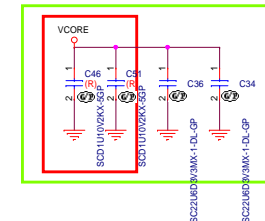


SB 1125 C340, C355 and C341 Allen modify

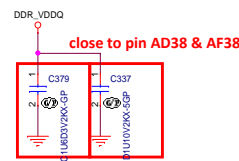
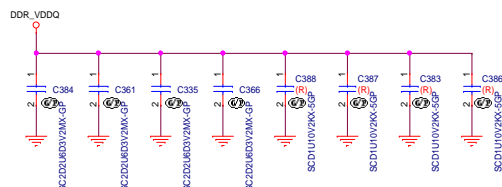


reserve the 0402 0.1u caps on reset for EMI(5/9).

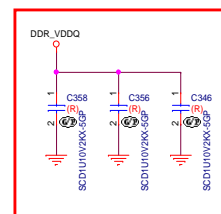
SB 1128 Allen modify



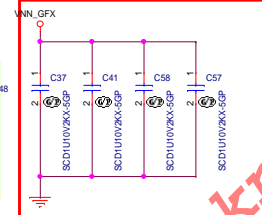
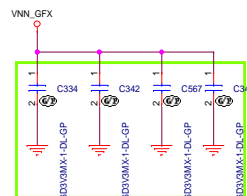
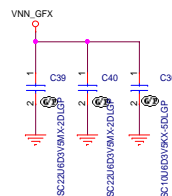
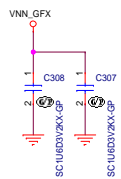
VDDQ_CPU



reserve the 0402 0.1u caps on reset for EMI(5/9).



VCOREG

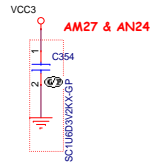


SB 1120 C334, C342, C348, C567 Allen modify

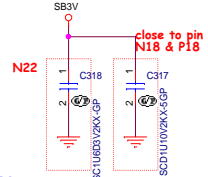
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1D0V_S0	1D0V_S0	12,15,43,44,45
1D0V_S5	1D0V_S5	15,44
1D05V_S0	1D05V_S0	15,43
1D5V_S0	1D5V_S0	15,31,34,43
1D8V_S0	1D8V_S0	10,12,13,15,19,23,25,30,35,38,43,46
1D8V_S5	1D8V_S5	12,15,20,23,28,30,34,38,43,44,56,57
1D35V_S0	1D35V_S0	15,42,43
V_3P3_A	V_3P3_A	12,20,23,35,38,40,46,47,57
VCC3	VCC3	12,13,15,20,21,23,24,25,30,31,34,35,36,38,39,46,56
SB3V	SB3V	12,15,20,30,34,35,38,43,44,45,47,48,57

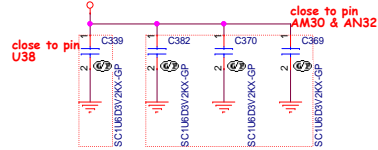
+3P3V_MAIN



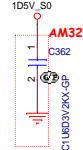
+3P3V_AUX



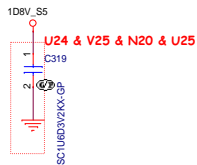
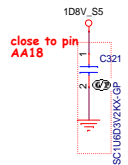
1D8V_S0



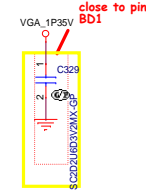
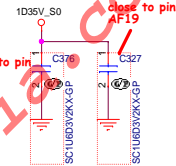
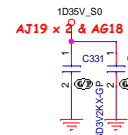
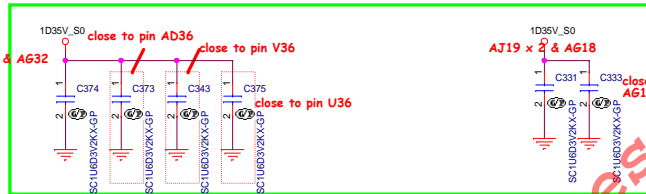
1D5V_S0



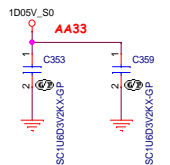
+1P8V_DUAL



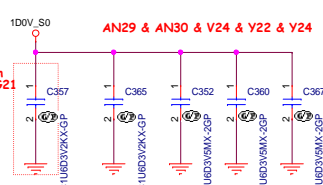
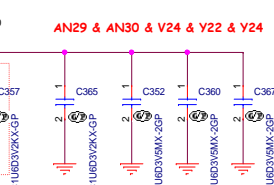
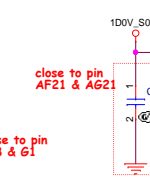
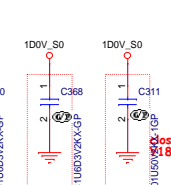
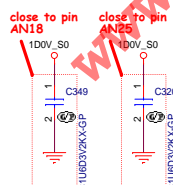
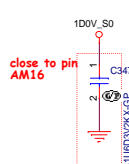
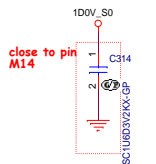
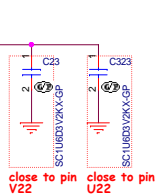
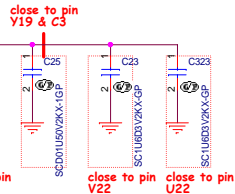
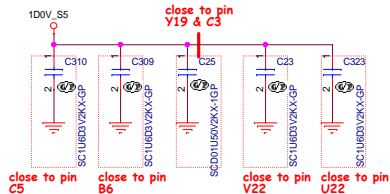
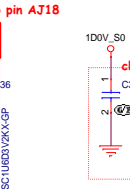
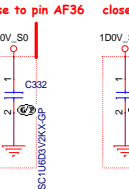
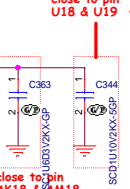
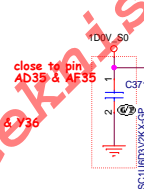
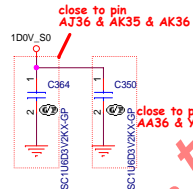
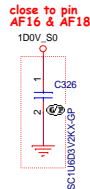
SB 1128 Allen modify

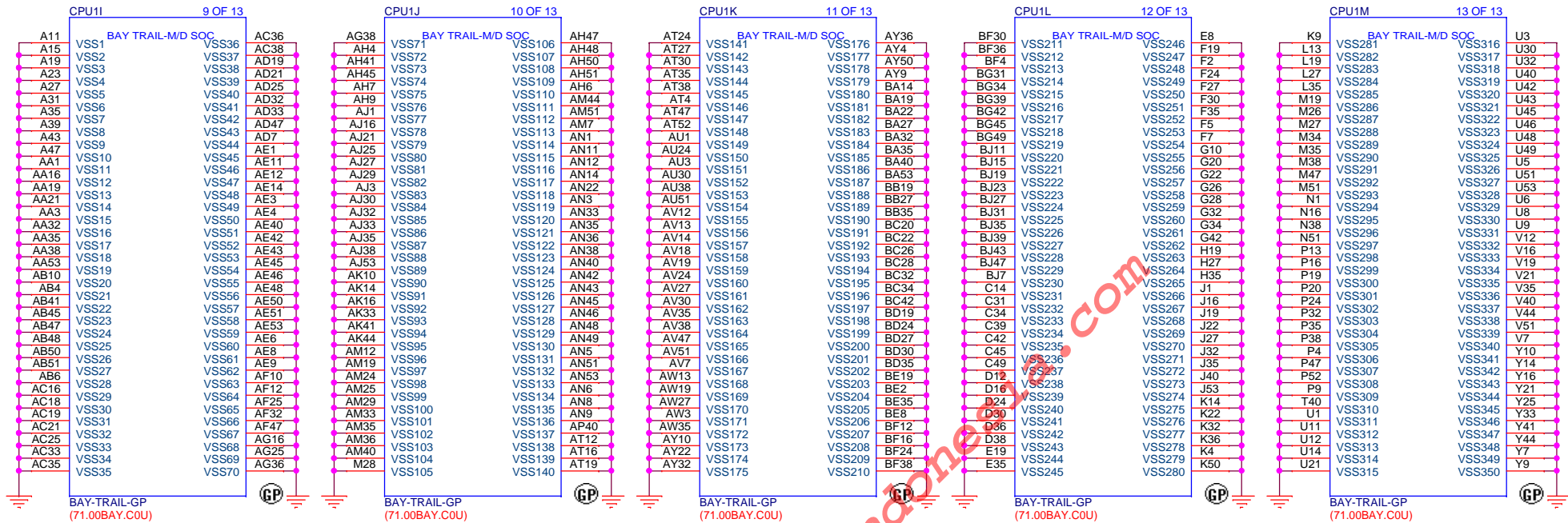


CRB 只放一顆 0.47uF



CRB 只放一顆 0.47uF





Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
CPU (VSS)

Size Document Number
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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDIO Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDIO_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDIO detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDIO not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

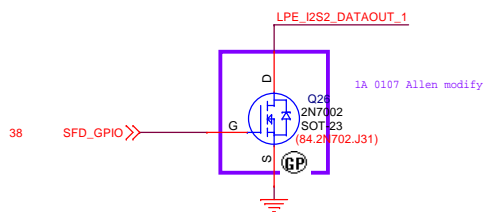
Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDIO_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDIO Detect 0 = DDIO not detected 1 = DDIO detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note:

The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.



DDR_0D675V 42
DDR_VDDQ 8,14,16,42,48
VCC3 12,13,15,17,19,23,24,25,30,31,34,35,36,38,39,46,56

DDR DATA

8 M_DATA_A0[63]
8 M_DQS_A_DP0[7]
8 M_MA_DM[7:0]

DDR CMD/ADD

8 M_MAA_A0[15]
8 M_WE_A_N
8 M_CAS_A_N
8 M_RAS_A_N
8 M_SBS_A0
8 M_SBS_A1
8 M_SBS_A2

DDR CTRL

8 M_SCS_A_N0
8 M_SCS_A_N1
8 M_SCKE_A0
8 M_SCKE_A1
8 M_ODT_A0
8 M_ODT_A1

DDR CLOCK

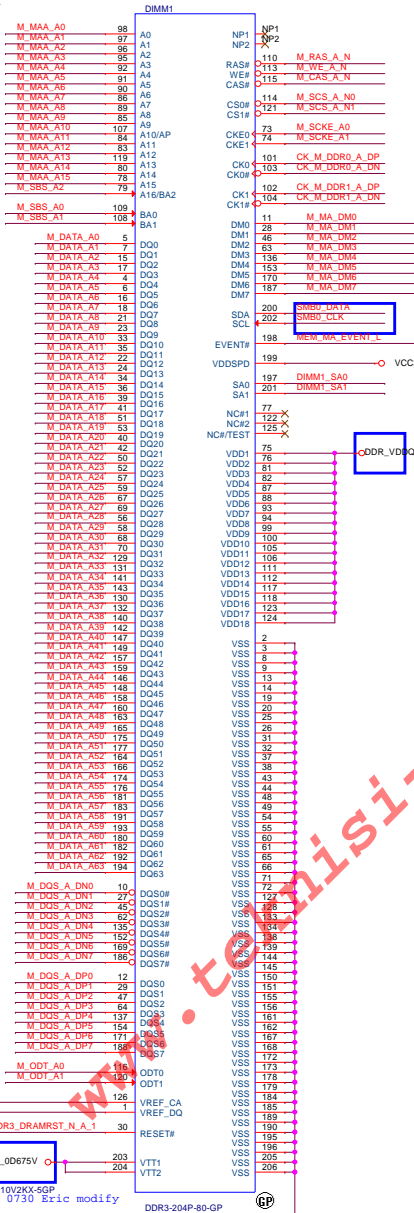
8 CK_M_DDR0_A_DP
8 CK_M_DDR0_A_DN
8 CK_M_DDR1_A_DP
8 CK_M_DDR1_A_DN

DDR OTHERS

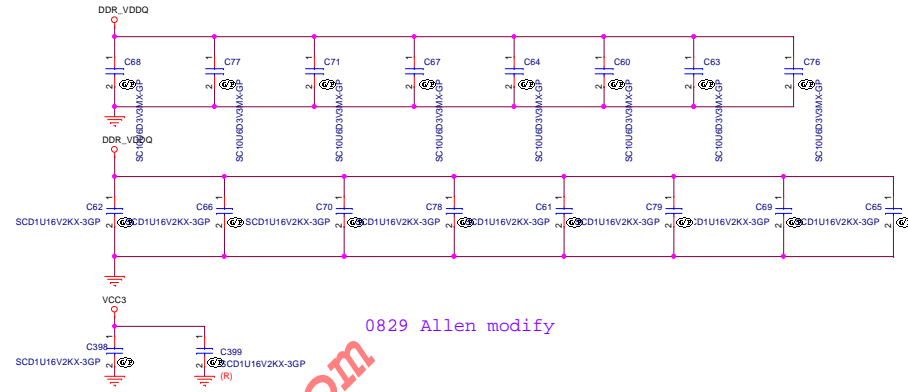
8 DDR3_DRAMRST_N
13,23,38,52 SMB0_CLK
13,23,38,52 SMB0_DATA

8 SIO_MEM_EVENT_L

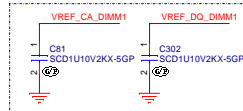
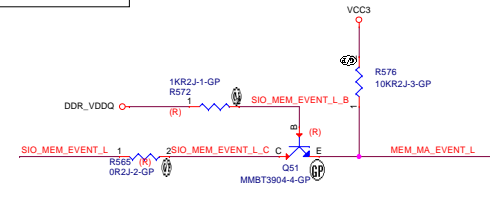
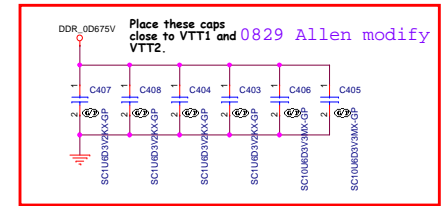
0524 0613 Eric change DIMM connector back



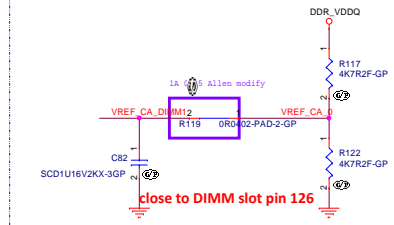
Note:
If SA0 DIM0 = 0, SA1 DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 0, SA1 DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



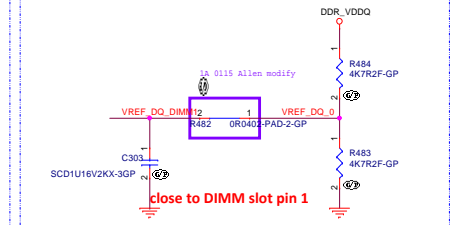
0829 Allen modify



For Intel Recommend Close to DIMM1 (Bay Trail)

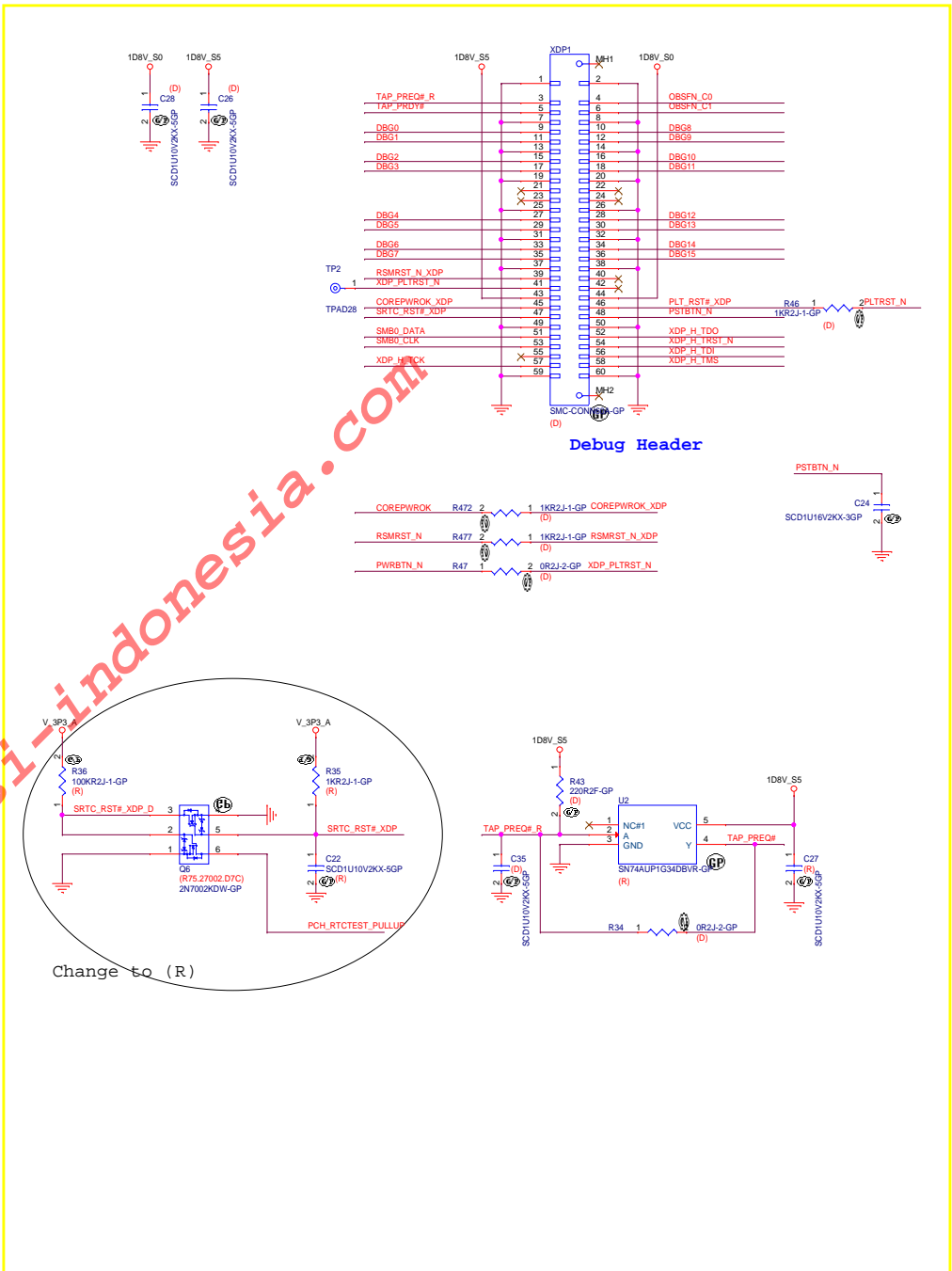
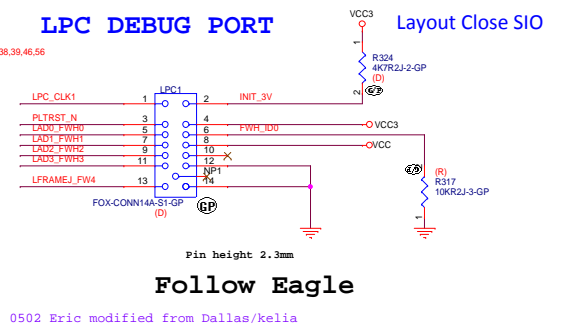
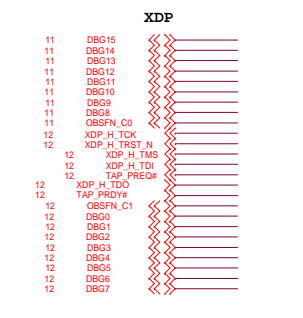
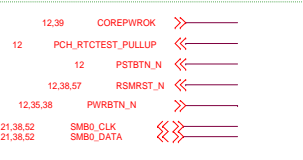
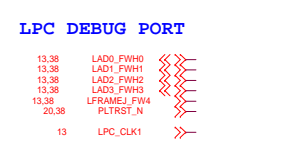


For Intel Recommend Close to DIMM1 (Bay Trail)



<Variant Name>

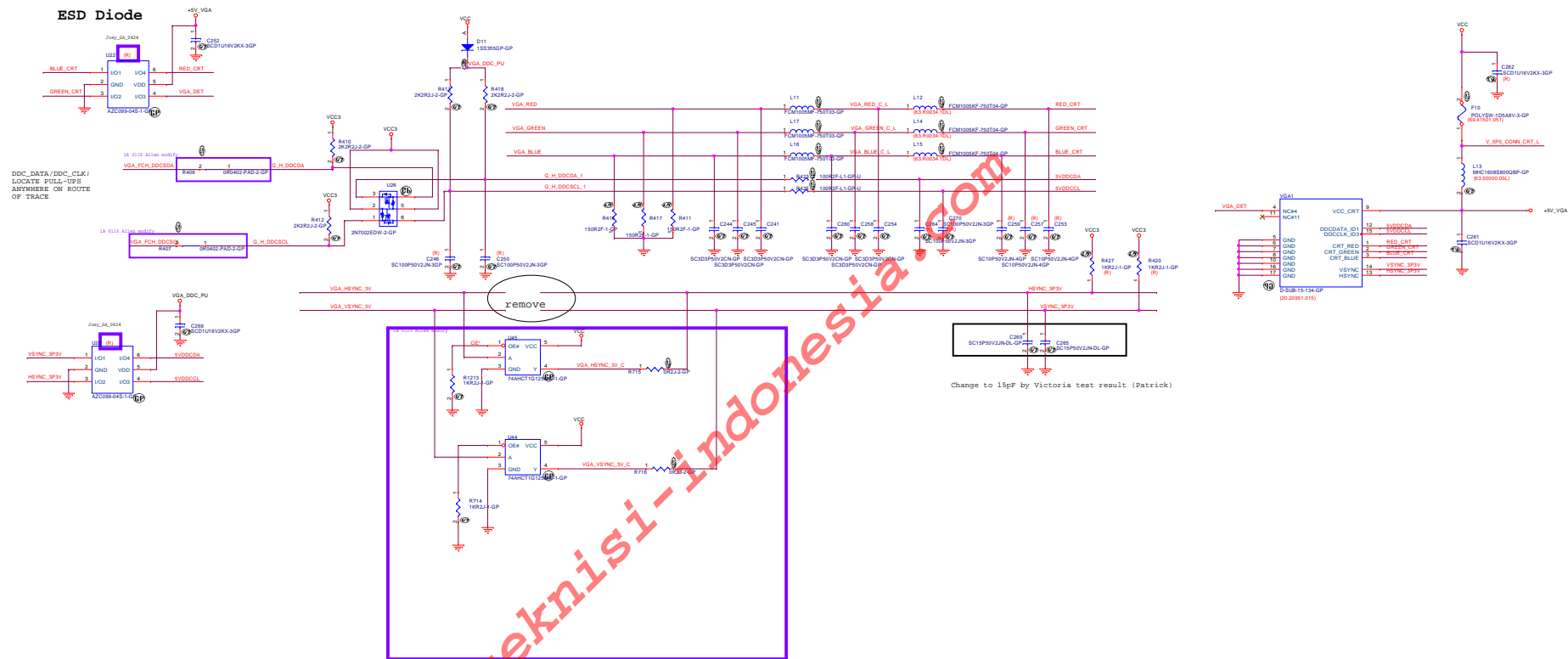
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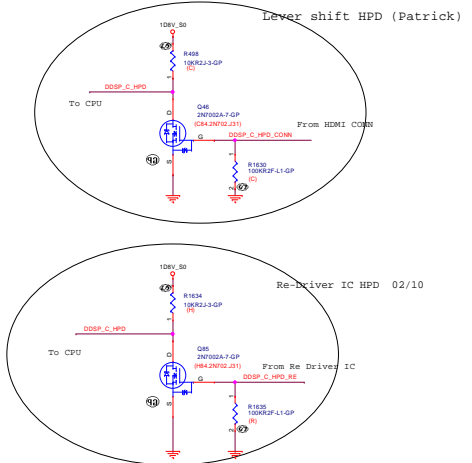
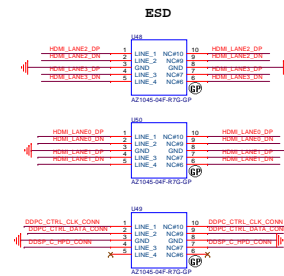
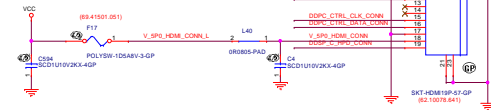


VCC 22,25,26 10,30,42,45,50,59
VCC3 12,13,17,18,21,23,25,30,31,34,35,36,38,39,46,58

Debug VGA

RGB	11	VGA_RED
	11	VGA_GREEN
	11	VGA_BLUE
SYNC	11	VGA_HSYNC_3V
	11	VGA_VSYNC_3V
DDC	11	VGA_FCH_DDCSDA
	11	VGA_FCH_DDCSCL
DETECT	38	VGA_DET



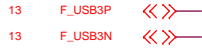


Remove DP to LVDS CIRCUIT

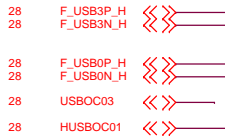
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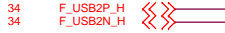
From CPU



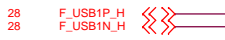
USB2.0 Front



USB2.0 BT



USB2.0 Card Reader

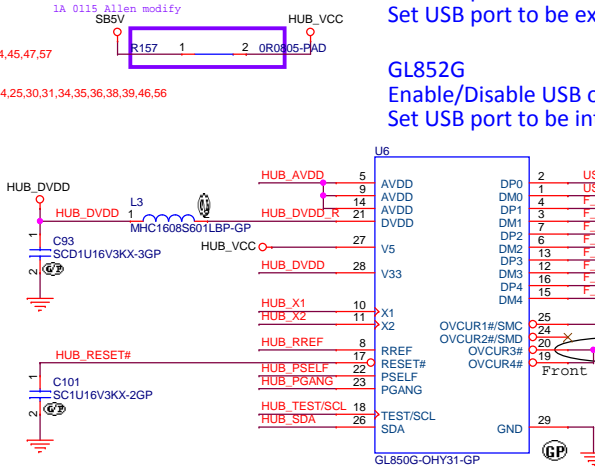


GL850G

Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
Set USB port to be internal (non-removable): set OC pin is floating
Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

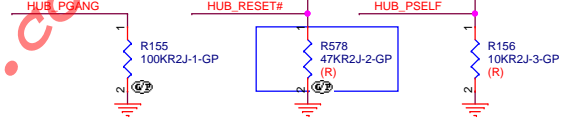
GL852G

Enable/Disable USB output port: setting by EEPROM
Set USB port to be internal (non-removable) or external (removable): setting by EEPROM



USB2.0 Card Reader DP+/D-
USB2.0 BT DP+/D-
USB2.0 Front DP+/D-, 3

Individual Mode



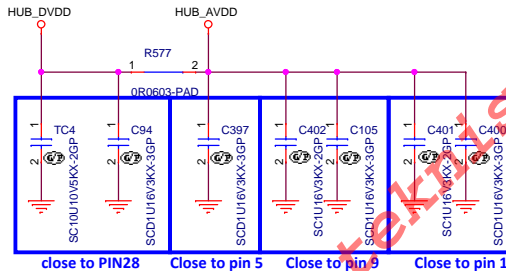
HUB_PSELF = 1 if self-powered
HUB_PSELF = 0 if bus-powered

Co-lay GL850G and GL852G

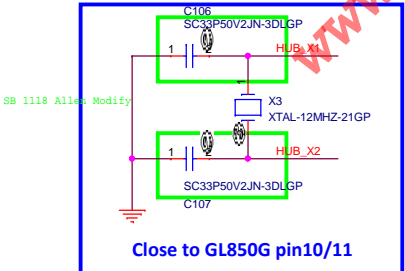
GL850G: 71.0850G.003 (USB2.0 STT 1 to 4)
GL852G: 71.00852.A03 (USB2.0 MTT 1 to 4)

Internal Power

(Hub Internal VR output from pin 28 V33 = HUB_DVDD)

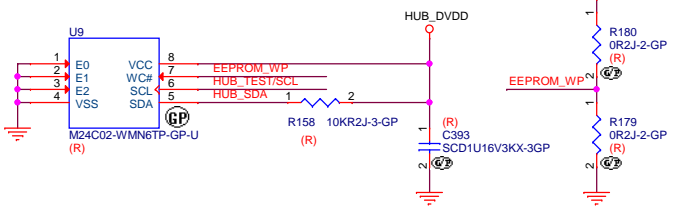


Xtal accuracy: +/- 20ppm



EEPROM

EEPROM is used for customized VID, PID, String, Configuration
The purpose is to set 4 USB ports to be internal/external
Default settings: 4 ports are external ports



Remove Card Reader

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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
NA

Size
B

Document Number
Rosa_BayTrail_DT

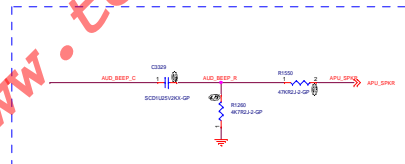
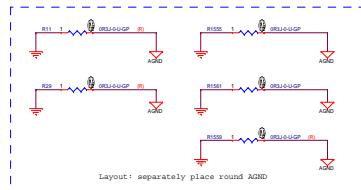
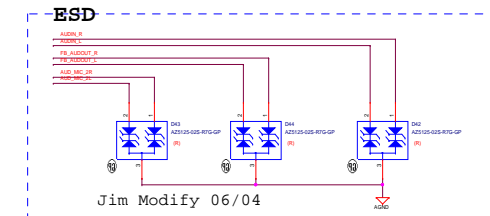
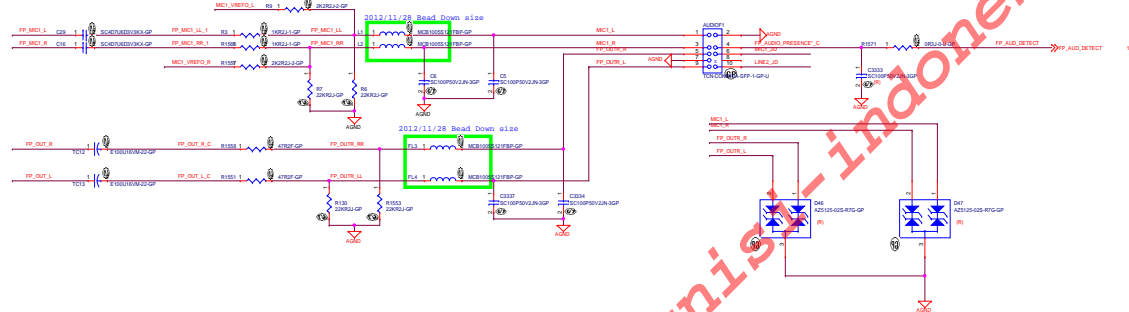
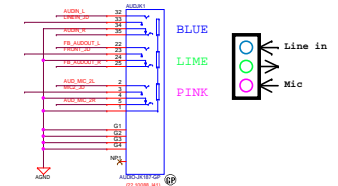
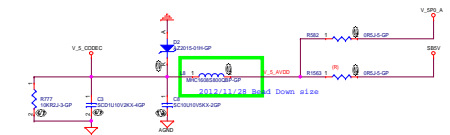
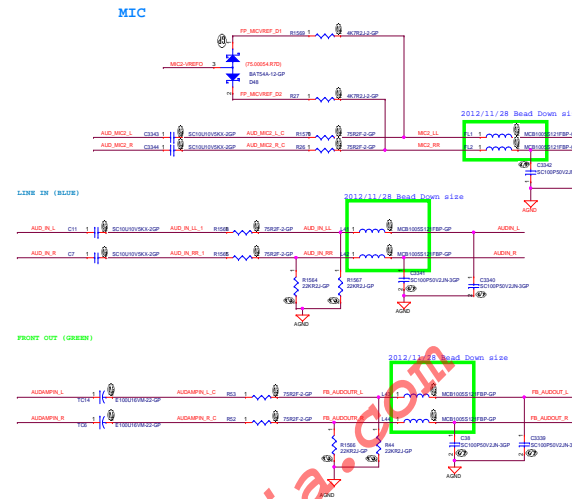
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A00

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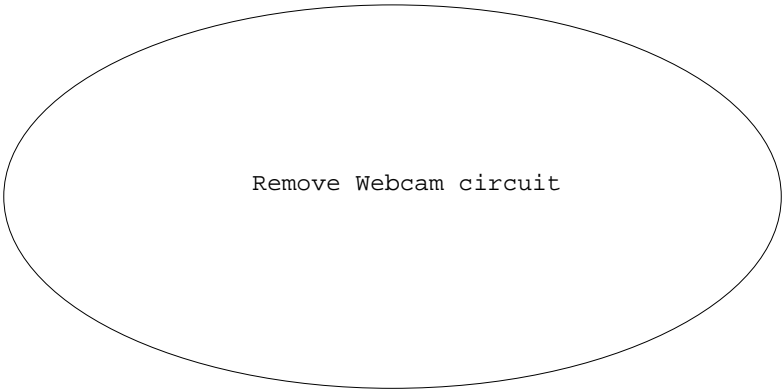


From APU



Remove AMP circuit

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Remove Webcam circuit

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1D5V_S0 15,17,31,43
SB3V 12,15,17,20,30,35,38,43,44,45,47,48,57
1D8V_S5 12,15,17,20,23,28,30,38,43,44,56,57
VCC3 12,13,15,17,20,21,23,24,26,30,31,35,36,38,39,46,56

0515 Eric modify net name

Wireless Card

12 CK_PCIE1_WLAN_DN
12 CK_PCIE1_WLAN_DP

From USB HUB

27 F_USB2N_H
27 F_USB2P_H
10 HSO_C_DN2 From PCH...TX
10 HSO_C_DP2 From PCH...TX
10 HSL_C_DN2 From PCH...RX
10 HSL_C_DP2 From PCH...RX

20,30 WAKE_N

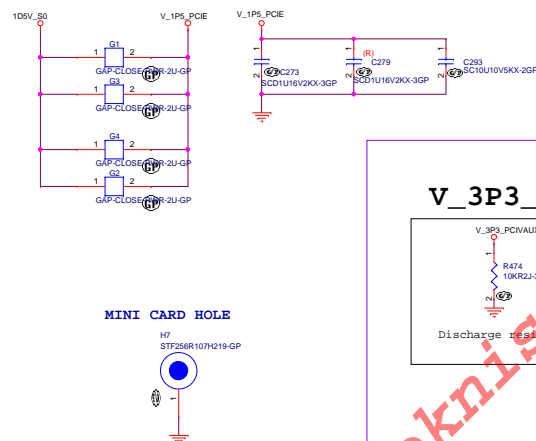
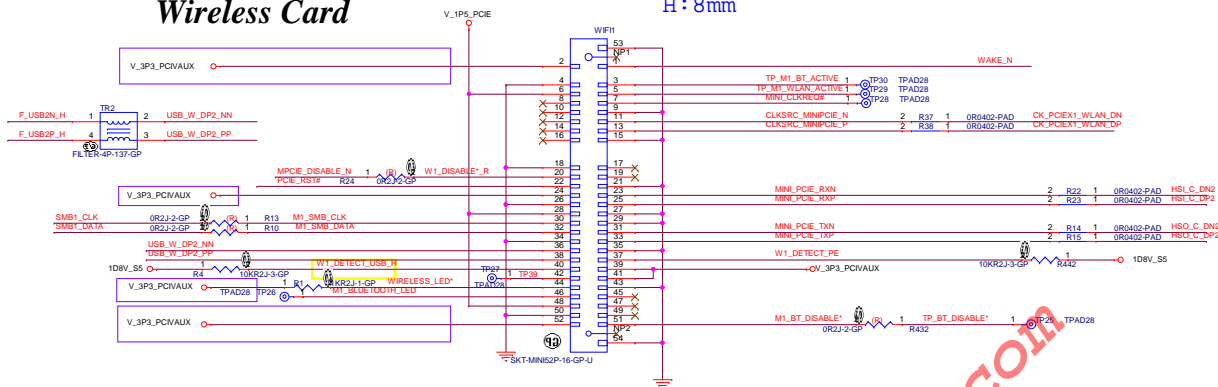
38 SMB1_CLK
38 SMB1_DATA

PCH_GPIO

38 PCIE_RST#
38 MPCIE_DISABLE_N
38 Mini_Power_CTRL
12 W1_DETECT_USB_H
12 W1_DETECT_USB_H
12 W1_DETECT_PE
12 W1_DETECT_PE

Wireless Card

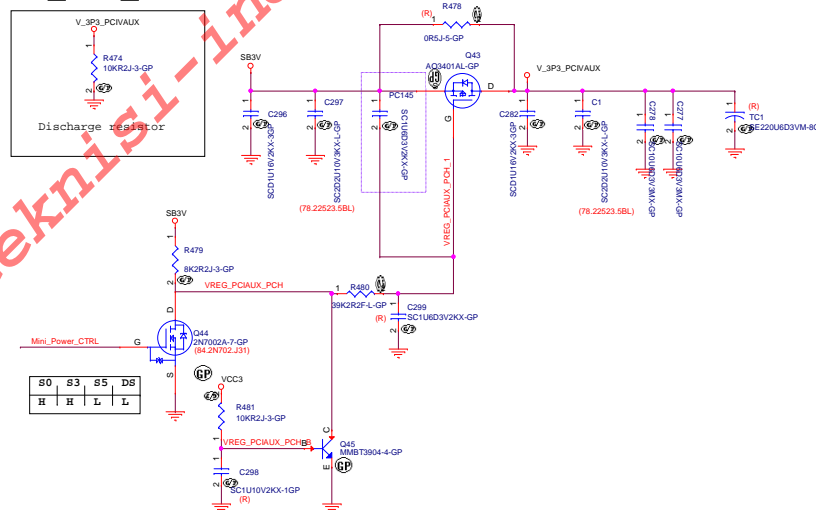
H: 8mm



MINI CARD HOLE



V_3P3_PCIVAUX DUAL



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Haichih, Taipei

Title WIRELESS BT

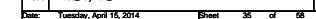
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Customer: Ray/Tai_DT

Date: Tuesday, April 15, 2014

Rev Add

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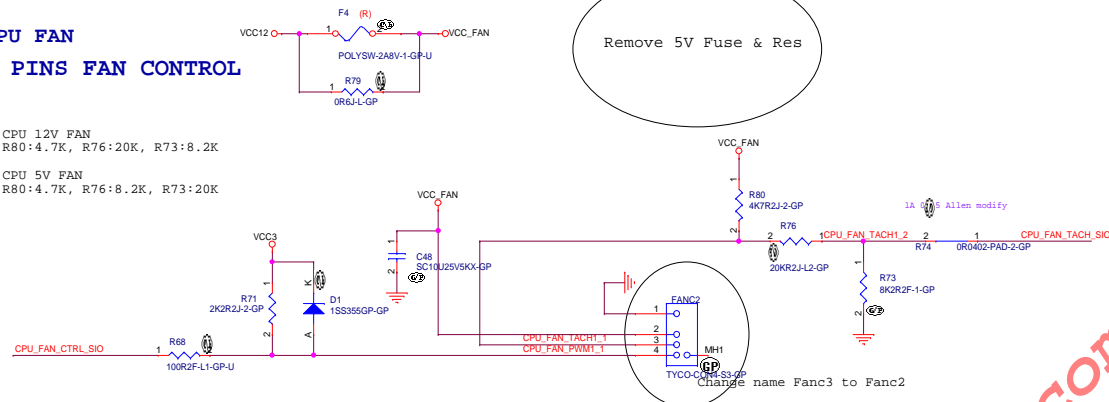
VCC3 <<> VCC3 12,13,15,17,20,21,23,24,25,30,31,34,35,36,38,46,56
VCC12 <<> VCC12 35,38,41

CPU FAN 4 PINS FAN CONTROL

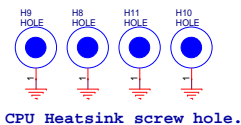
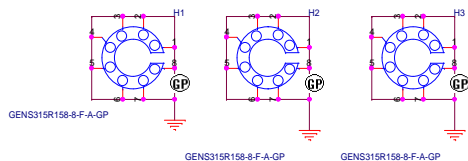
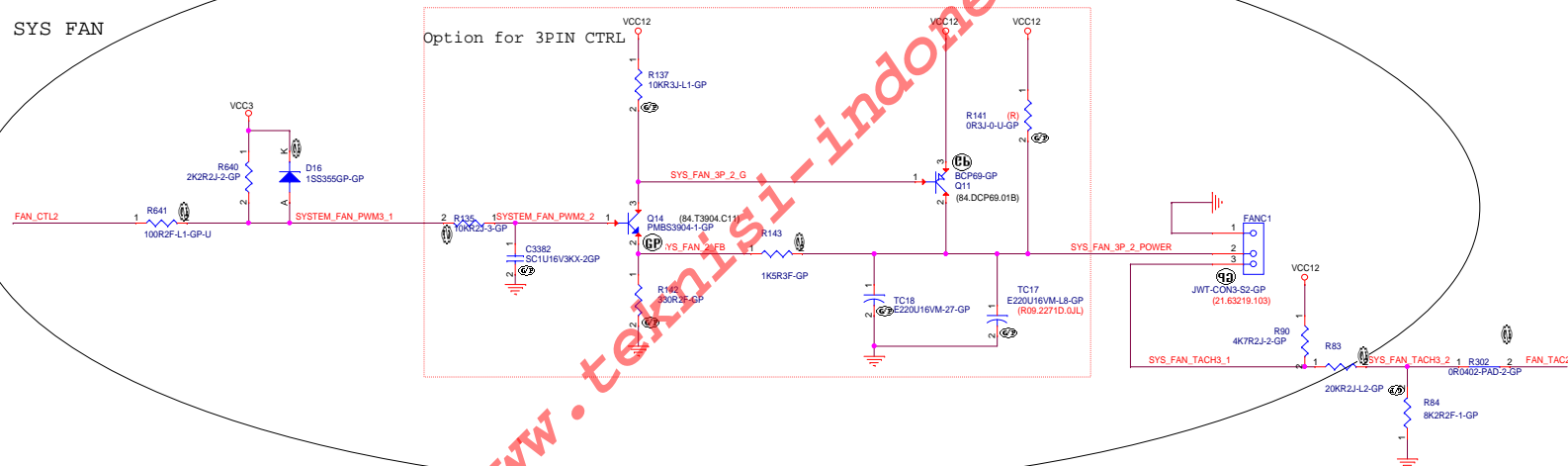
CPU 12V FAN
R80:4.7K, R76:20K, R73:8.2K
CPU 5V FAN
R80:4.7K, R76:8.2K, R73:20K

SIO FAN CONTROL

38 CPU_FAN_CTRL_SIO <<>
38 CPU_FAN_TACH_SIO <<>
38 FAN_TAC2 <<>
38 FAN_CTL2 <<>



SYS FAN



CPU Heatsink screw hole.

BY vendor 不接任何gnd, 以防noise cover audio

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title FAN CIRCUITS/HOLE

Size C Document Number
Rosa_BayTrail_DT


Rev
A00

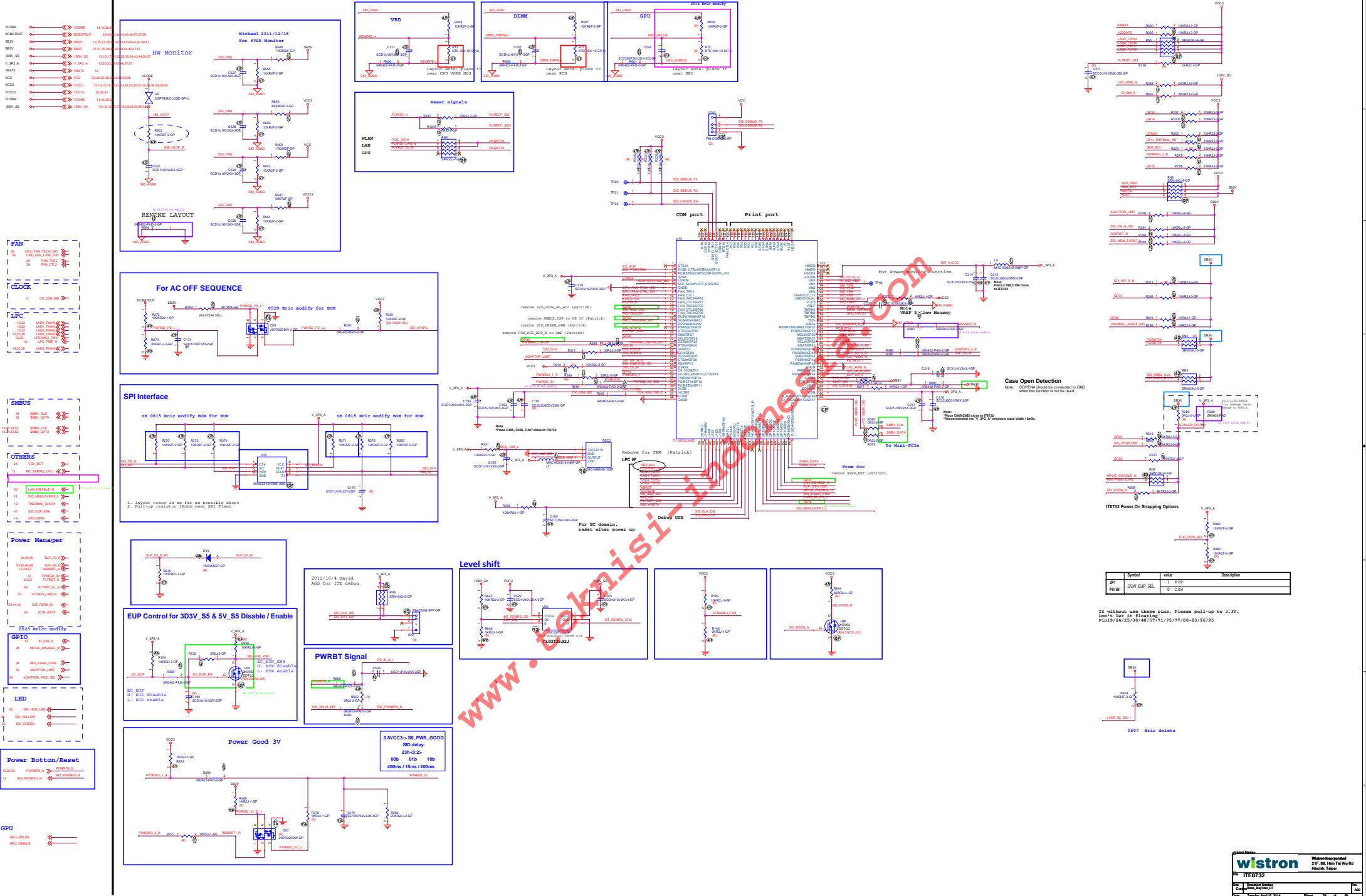
Date: Tuesday, April 15, 2014

Sheet 36 of 58

Remove TPM Function

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<Variant Name>		
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TPM		
Size	Document Number	Rev
CustomRose_BayTrail_DT		A00
Date:	Tuesday, April 15, 2014	Sheet 37 of 58



Symbol	value	Description
J1	DSW_EUP_SEL	1 STOP
Pin 10	0	DSW

If without use these pins, Please pull-up to 3.3V.
Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80-83/96/99



DCBATOUT 38.30,41,42,43,45,46,47,57,58

V_3PS_A 13.20,23,25,30,46,47,57

V_5PS_A 26,30,31,46,47

DCBATOUT PWR_3_5V_DCBATOUT

PR100 1 2 0R000-PAD

PR101 1 2 0R000-PAD

PR102 1 2 0R000-PAD

UG-84.08884.B37 FDS8884

Vgs @ 4.5V,

Id = 7.5A,

Rds(on) = 30.0mohm,

Qg = 5.0-7.0nC

LG-84.06690.G37 FDS6690AS

Vgs @ 4.5V,

Id = 10A,

Rds(on) = 15.0mohm,

Qg = 9.0-13nC

UG-84.08884.B37 FDS8884

Vgs @ 4.5V,

Id = 7.5A,

Rds(on) = 30.0mohm,

Qg = 5.0-7.0nC

LG-84.06690.G37 FDS6690AS

Vgs @ 4.5V,

Id = 10A,

Rds(on) = 15.0mohm,

Qg = 9.0-13nC

VIN RIPPLE CURRENT I_{max}=0.95A

VIN RIPPLE CURRENT I_{max}=2.9A

I_{max}=2.5A

OCP>3.75A

Freq=375KHz

I_{max}=6.5A

OCP>10A

Freq=321KHz

V_3PS_A

PR1421 2 0R000-PAD

PR1461 2 0R000-PAD

PR1431 2 0R000-PAD

V_5PS_A

PR1041 2 0R000-PAD

PR1061 2 0R000-PAD

PR1021 2 0R000-PAD

3.3V(RT8243B)

L=3.3uH

$\Delta I = \frac{(V_{in}-V_{out}) \cdot V_{out}}{(V_{in} \cdot L \cdot F_{sw})}$

$\Delta I = \frac{(19 - 3.3) \cdot 3.3}{(19 \cdot 3.3 \cdot 375K)} = 2.2A$

5.08V(RT8243B)

L=3.3uH

$\Delta I = \frac{(V_{in}-V_{out}) \cdot V_{out}}{(V_{in} \cdot L \cdot F_{sw})}$

$\Delta I = \frac{(19 - 5.08) \cdot 5.08}{(19 \cdot 3.3 \cdot 320K)} = 3.52A$

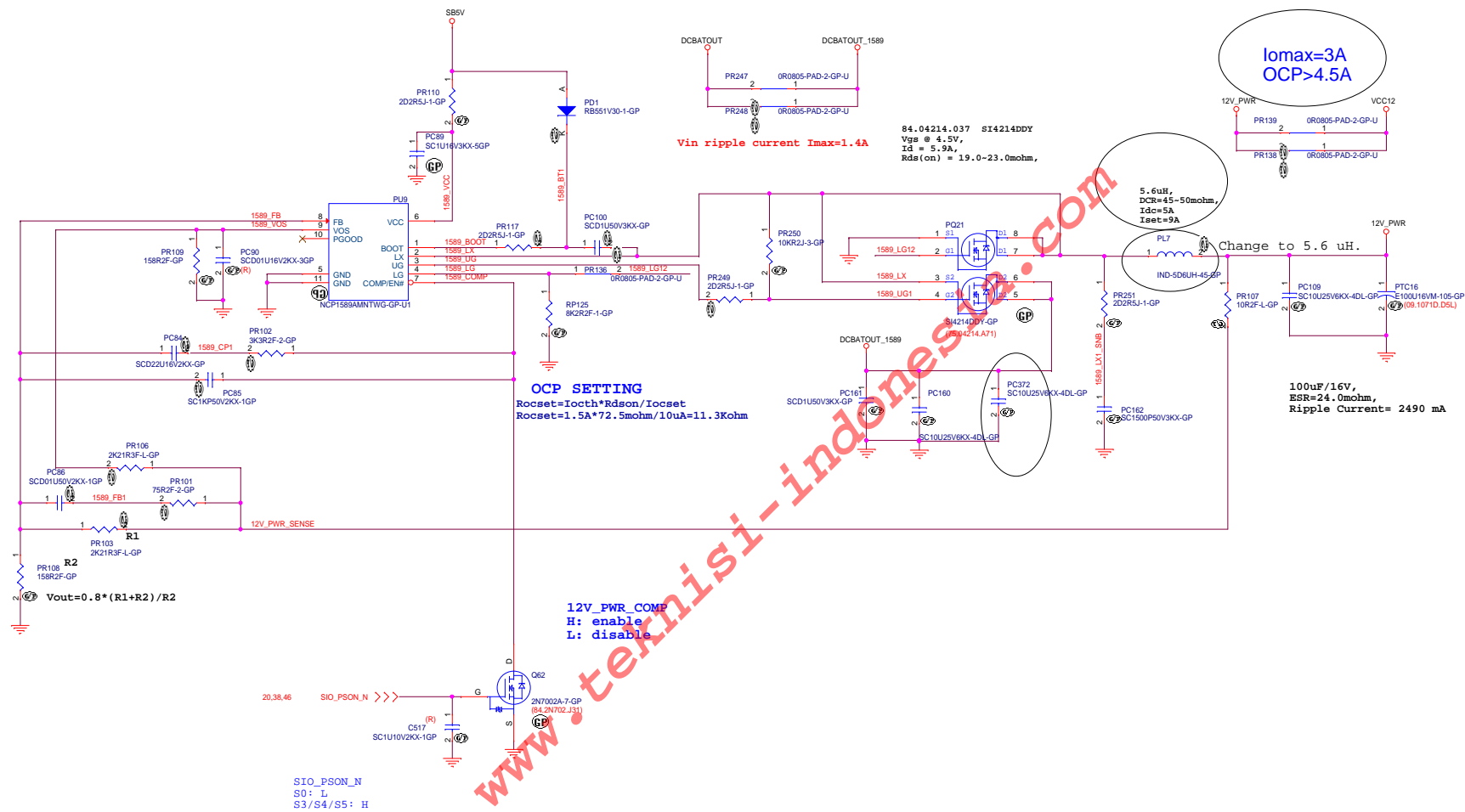
$V_0 = 2 \cdot \frac{(1 \cdot R_1 / R_2)}{1 + R_1 / R_2}$

$V_0(cal.) = 5.08V$

$V_0 = 2 \cdot \frac{(1 \cdot R_1 / R_2)}{1 + R_1 / R_2}$

$V_0(cal.) = 3.30V$

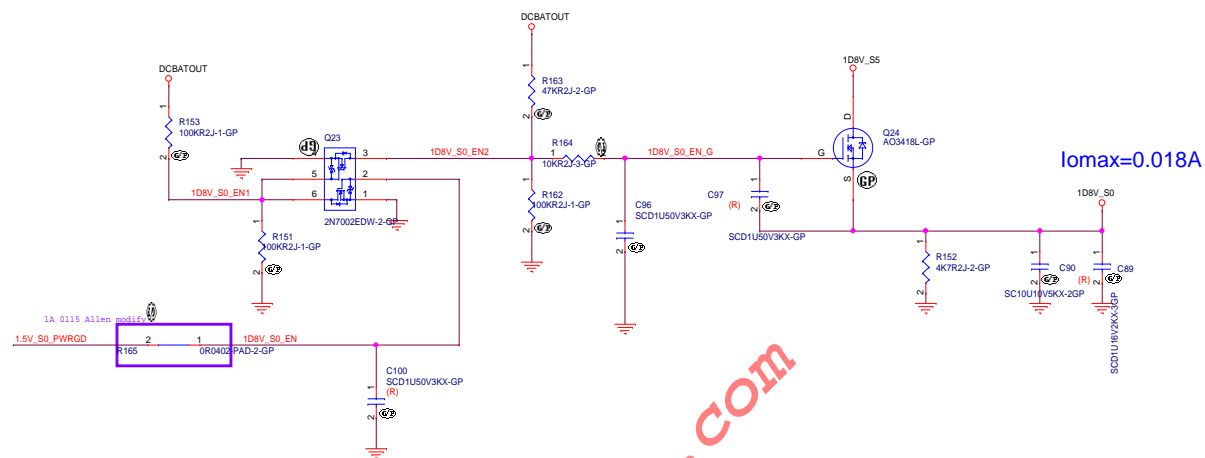
VCC12		VCC12	35,36,38
DCBATOUT		DCBATOUT	38,39,40,42,43,45,46,47,57,58
SB5V		SB5V	27,31,35,38,39,42,43,44,45,47,57



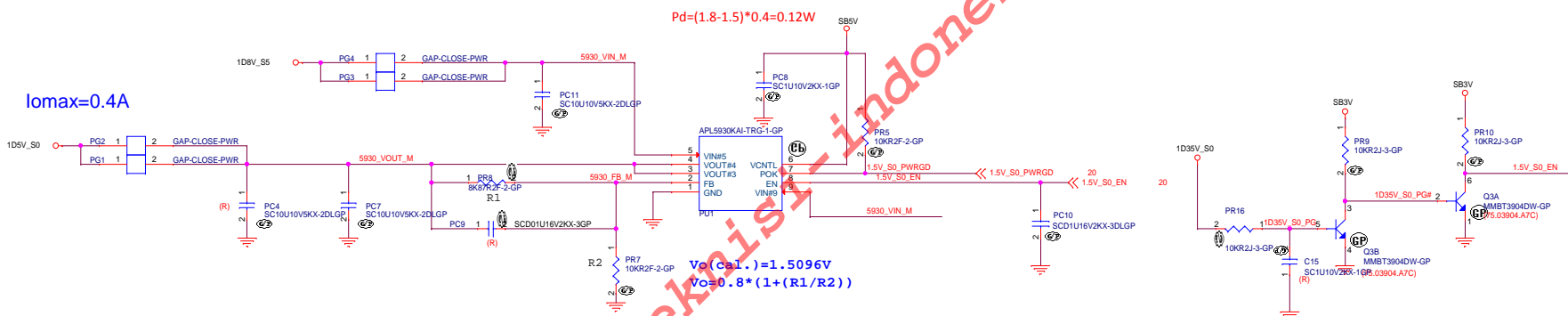


1D0V_S0	1D0V_S0	12,15,17,44,45
1D05V_S0	1D05V_S0	15,17
1D8V_S0	1D8V_S0	10,12,13,15,17,19,23,25,30,35,38,46
1D8V_S5	1D8V_S5	12,15,17,20,23,28,30,34,38,44,56,57
1D35V_S0	1D35V_S0	15,17,42
DCBATOUT	DCBATOUT	38,39,40,41,42,45,46,47,57,58
SB3V	SB3V	12,15,17,20,30,34,35,38,44,45,47,57
SB5V	SB5V	27,31,35,38,39,41,42,44,45,47,57
1D5V_S0	1D5V_S0	15,17,31,34

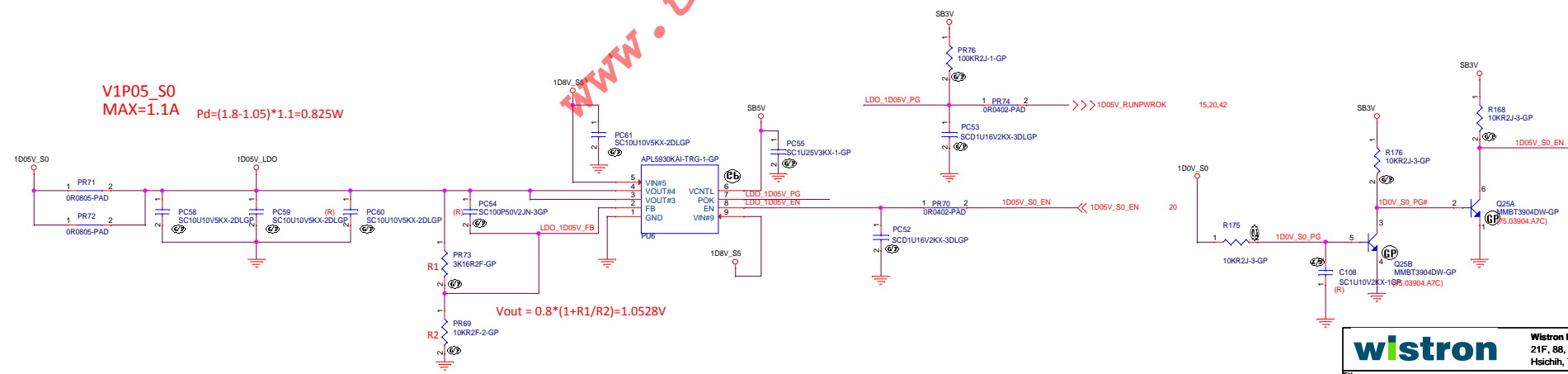
1.8V_S0

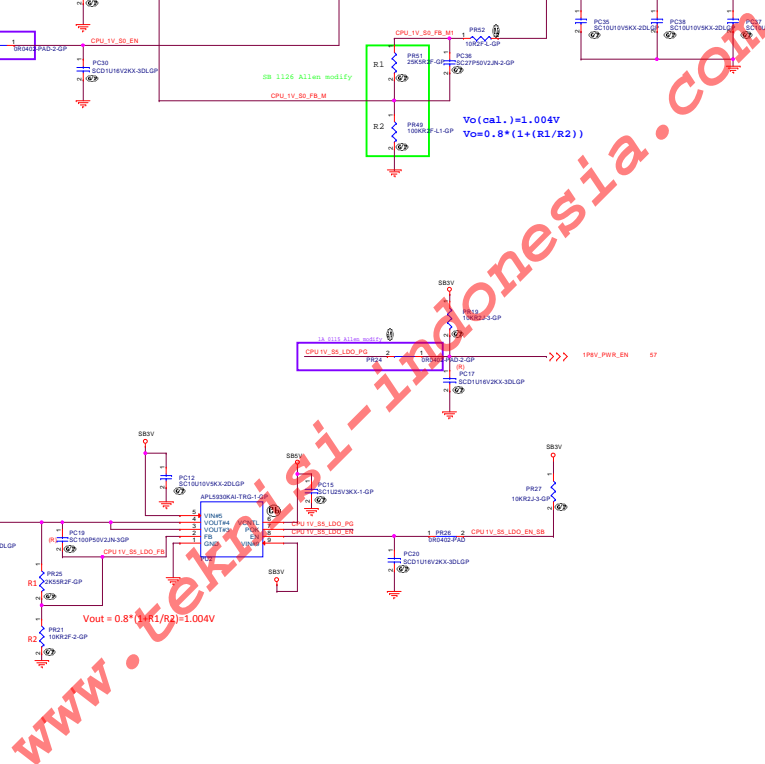


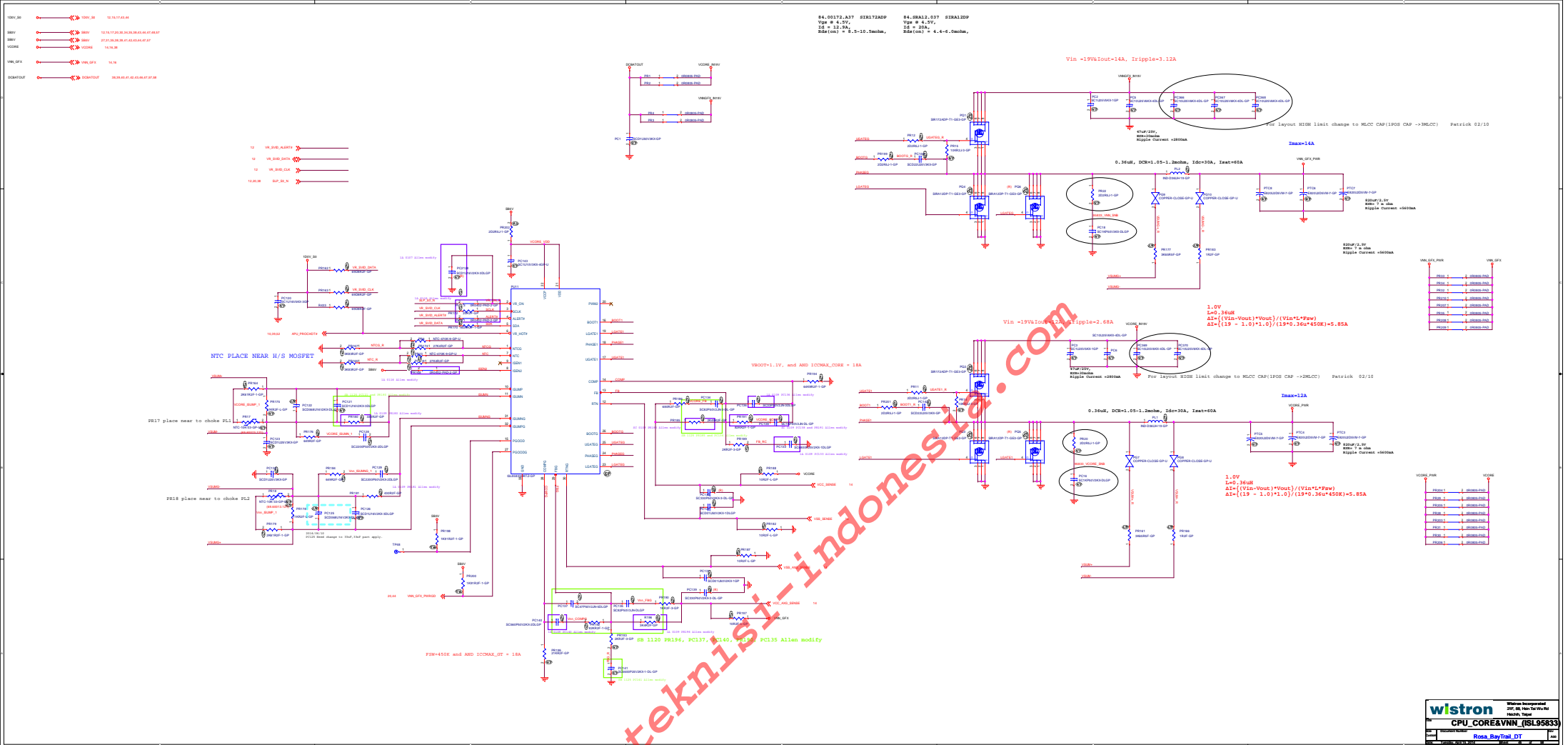
1.5V_S0

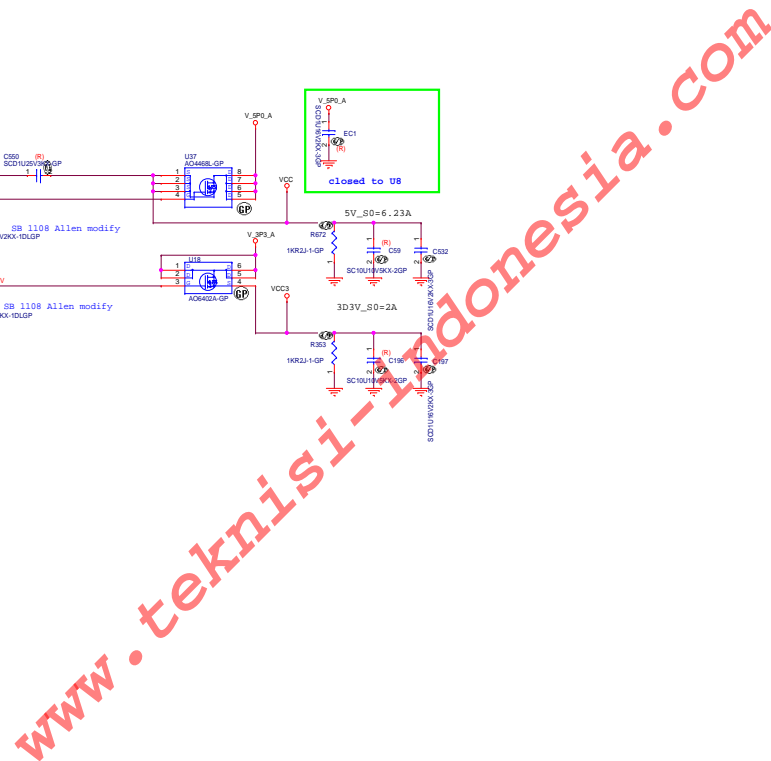
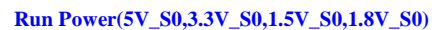


V1P05_S0
MAX=1.1A Pd=(1.8-1.05)*1.1=0.825W

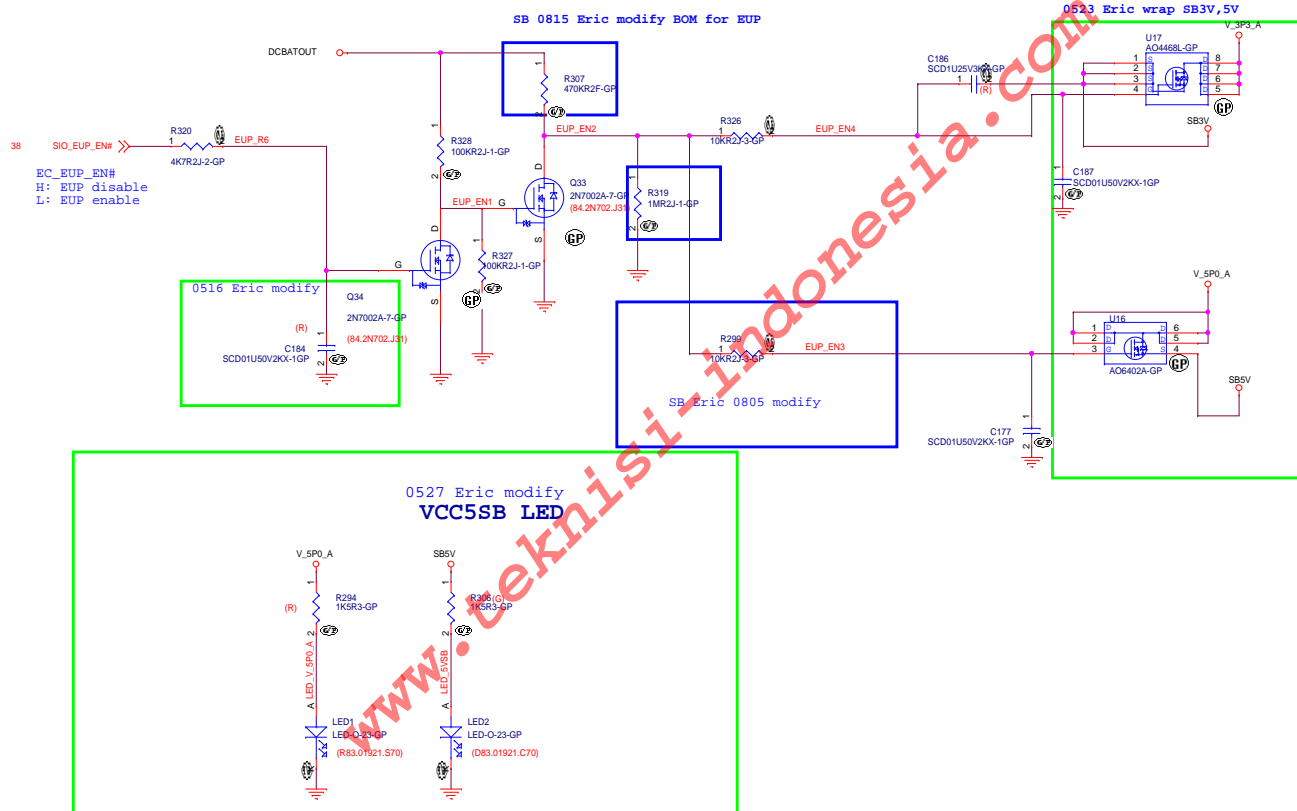


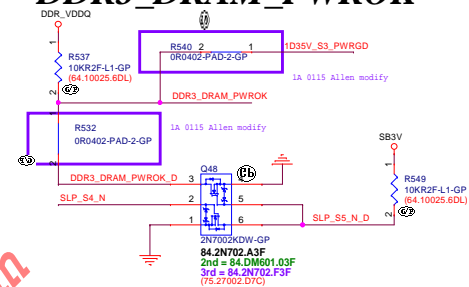
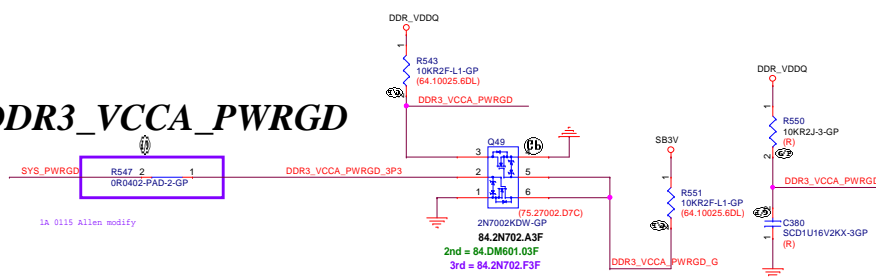




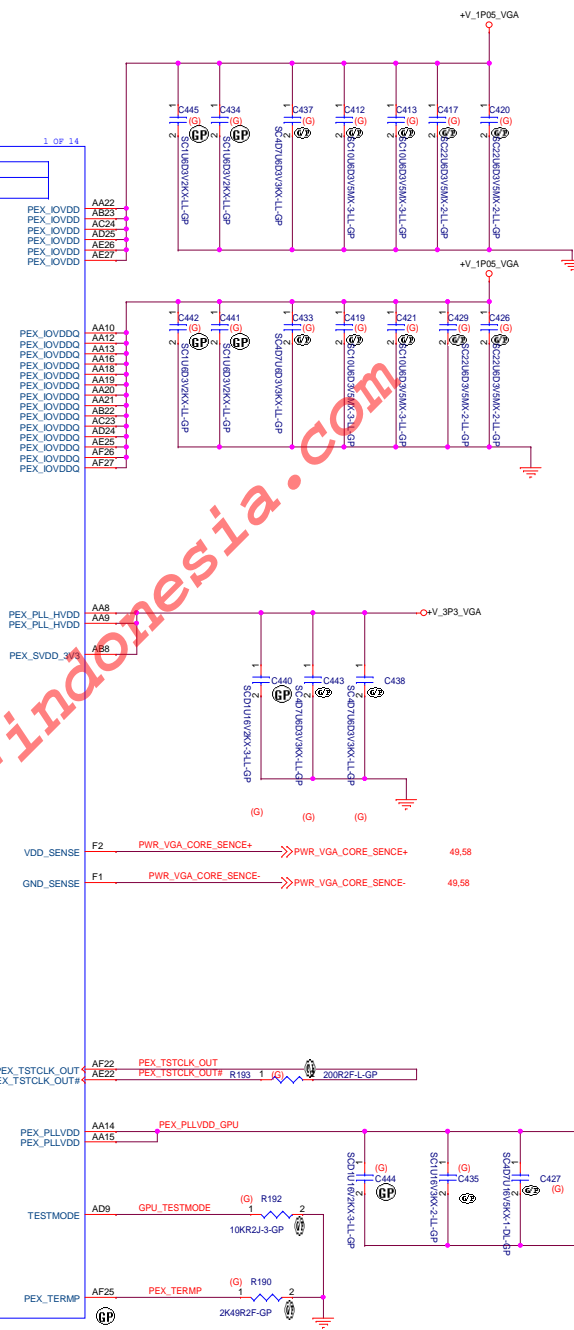
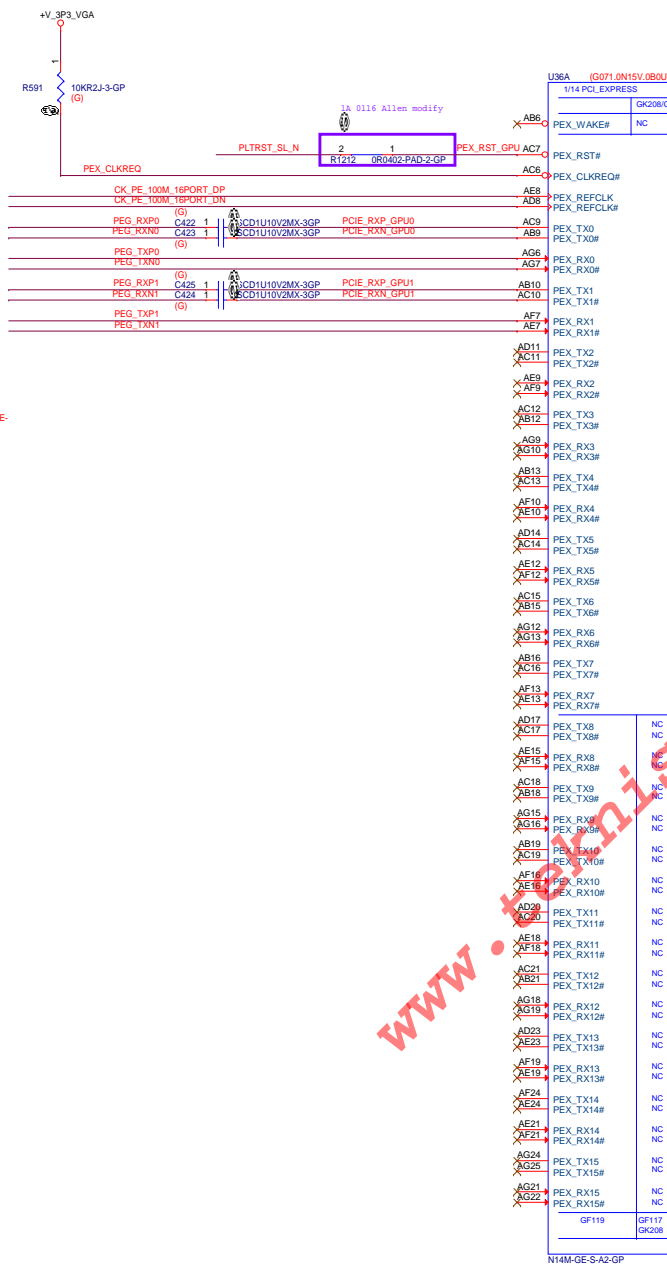


DCBATOUT	38,39,40,41,42,43,45,46,57,58
SB3V	12,15,17,20,30,34,35,38,43,44,45,48,57
SB5V	27,31,35,38,39,41,42,43,44,45,57
V_3P3_A	12,20,23,35,38,40,46,57
V_5P0_A	28,30,31,40,46

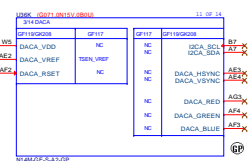
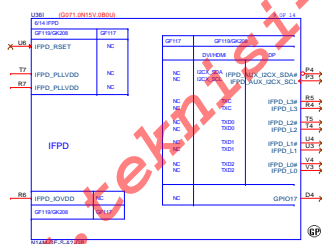


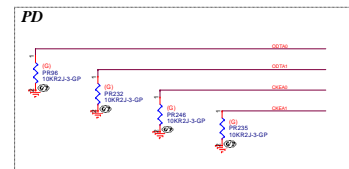
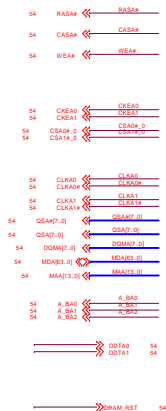


PCIEX2



Add two 1uF Caps according to the NV Comment





GF1XX SECDED CAC MAPPING			
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C001	0001		
C002	0002		
C003	0003		
C004	0004		
C005	0005		
C006	0006		
C007	0007		
C008	0008		
C009	0009		
C010	0010		
C011	0011		
C012	0012		
C013	0013		
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C015	0015		
C016	0016		
C017	0017		
C018	0018		
C019	0019		
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C423	0423		
C424	0424		
C425	0425		

* AllDs not required for any of 4 derivations, water up to 420s density

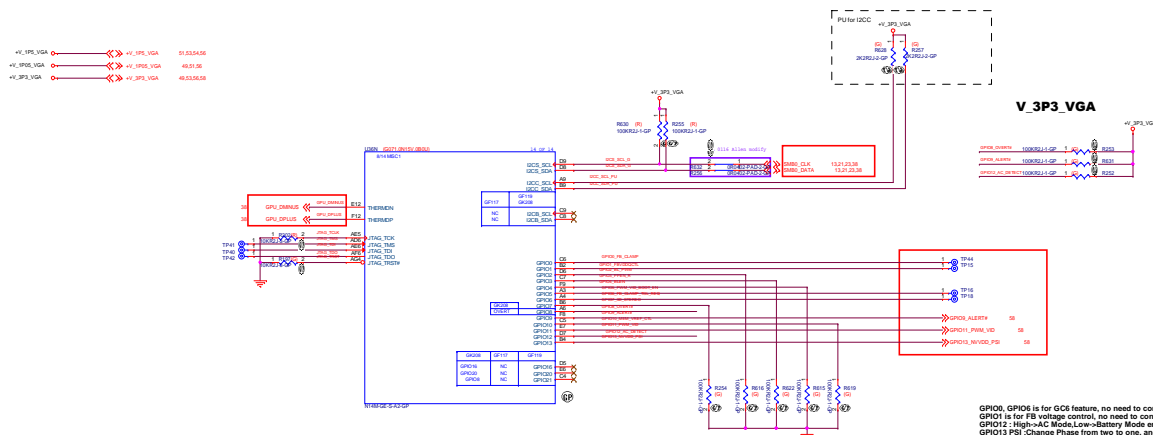


Table 115. G82-64 and GB4-128 GPIO Description

- GPIO20 and GPIO21 are only available on H14M-LP/-GS/-HE/-HS & H14P-GV/-GV2
- The greyed out section of Table 107 indicates GPIOs that are not available for H14M-GZ/-GL

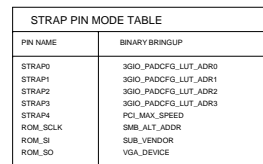


Table 122 Binary Strap Mode Mapping

Refer to the latest version of H14M-GE/ GL Memory Recommended Vendor List for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

Table 119. Device Specific Strap Mode Selection

XTAL

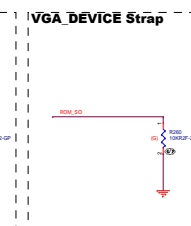
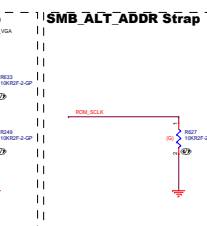
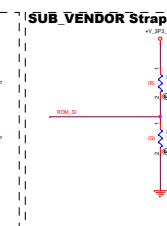
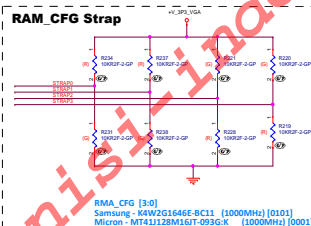
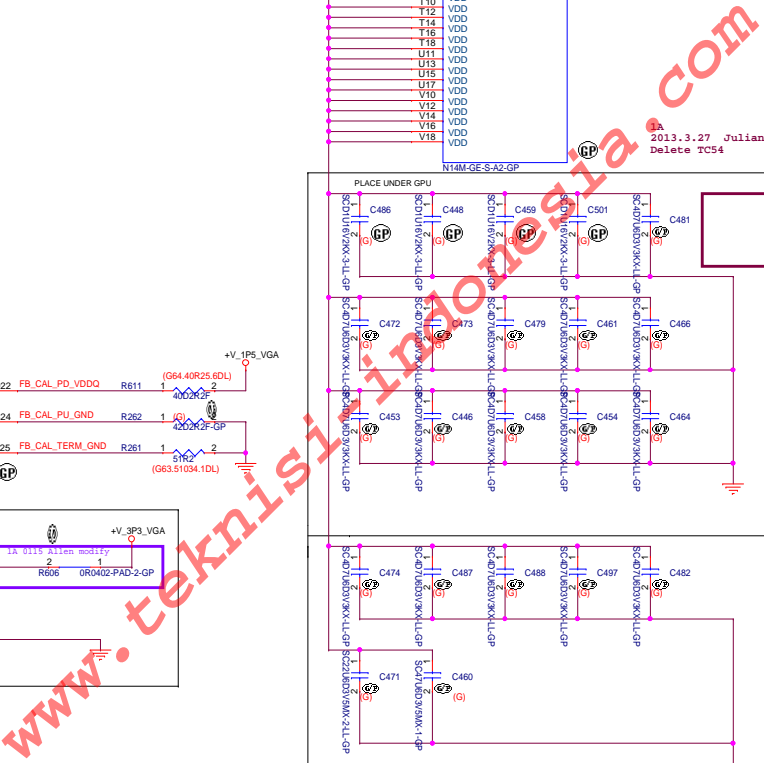


Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

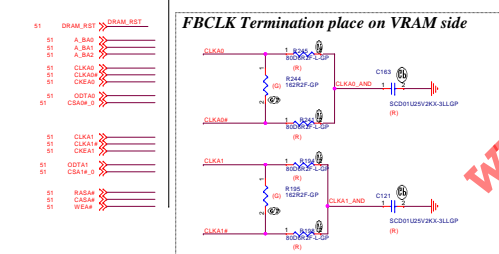
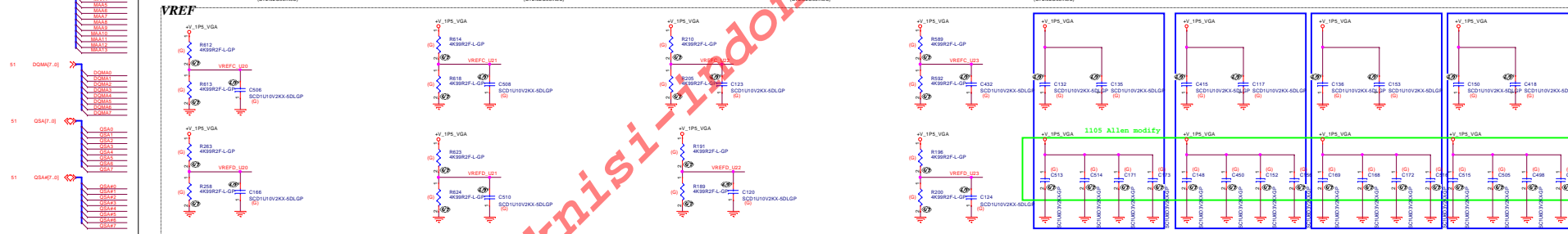
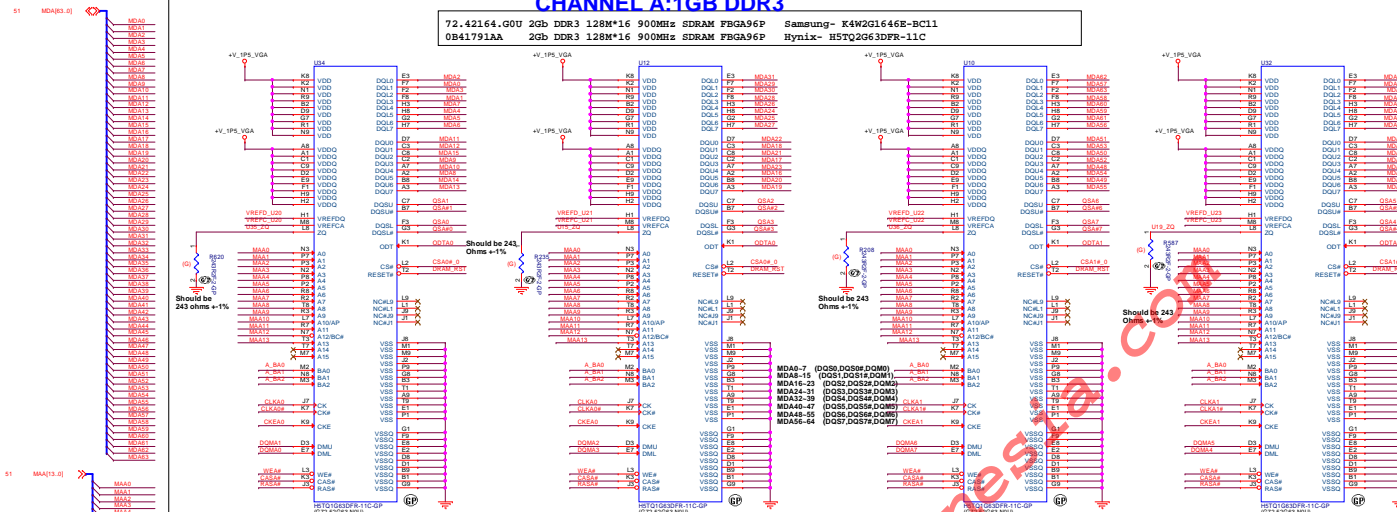
Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx1 Configuration



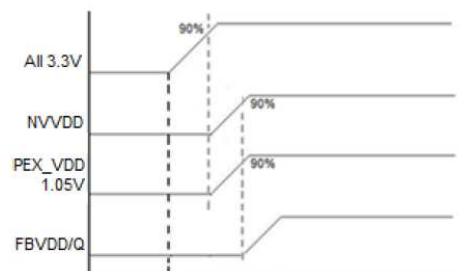
AV_1PS_VGA 0 4V_1PS_VGA 51.53.56
AV_1PS_VGA 0 4V_1PS_VGA 48.51.52.56

CHANNEL A:1GB DDR3

72.42164.G0U 2Gb DDR3 128M*16 900MHz SDRAM FBGA96P Samsung- K4W2G1646E-BC11
0B41791AA 2Gb DDR3 128M*16 900MHz SDRAM FBGA96P Hynix- H5TQ2G63DFR-11C



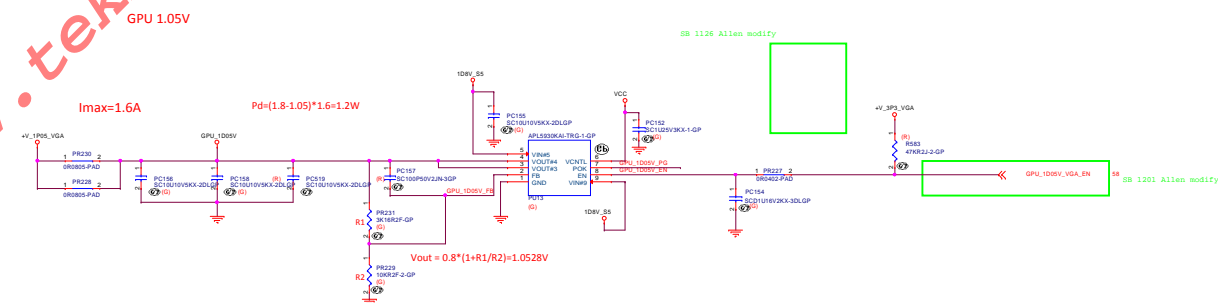
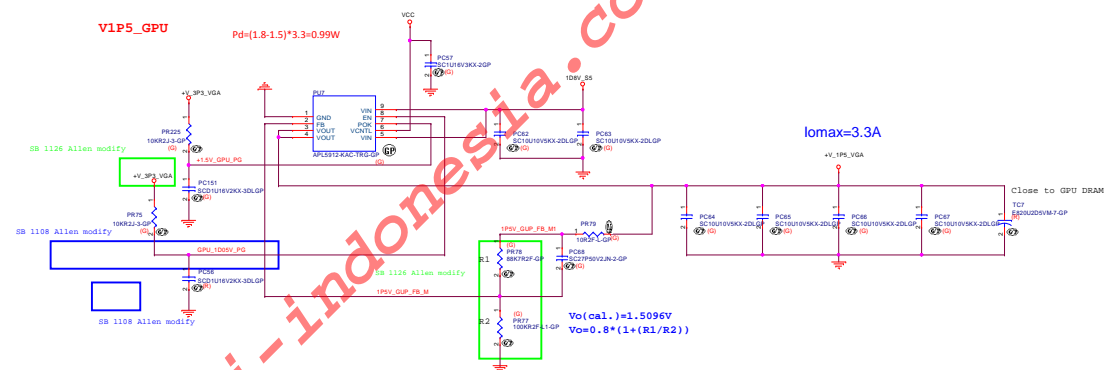
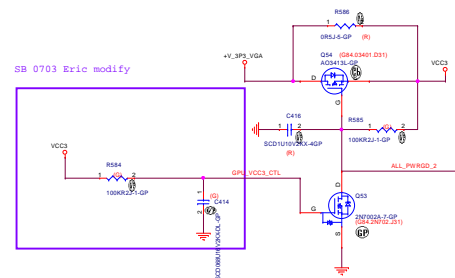
3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

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3D3V_S0 to 3D3V_DELAY Transfer



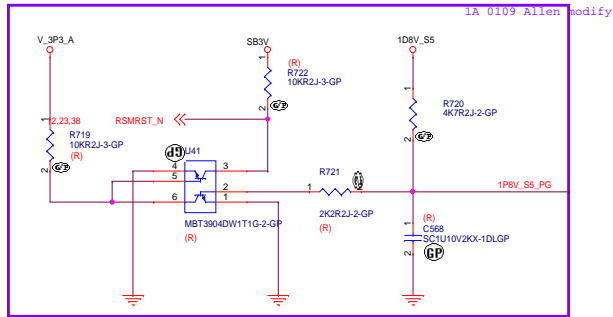
1D8V_S5 <<> 1D8V_S5 12,15,17,20,23,28,30,34,38,43,44,56

DCBATOUT <<> DCBATOUT 38,39,40,41,42,43,45,46,47,58

SB3V <<> SB3V 12,15,17,20,30,34,35,38,43,44,45,47,48

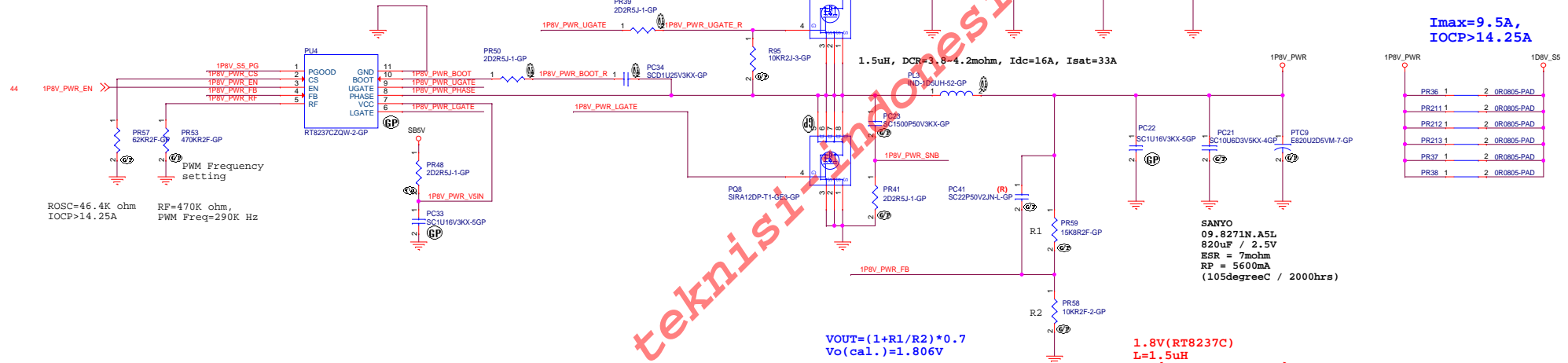
SB5V <<> SB5V 27,31,35,38,39,41,42,43,44,45,47

V_3P3_A <<> V_3P3_A 12,20,23,35,38,40,46,47



84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5-10.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4-6.0mohm,



+V_3P3_VGA <-> +V_3P3_VGA 49.52,53.56
 +V_VGA_CORE <-> +V_VGA_CORE 53
 DCBATOUT <-> DCBATOUT 38.39,40,41,42,43,45,46,47,57
 VCC <-> VCC 23,24,25,38,39,42,48,56

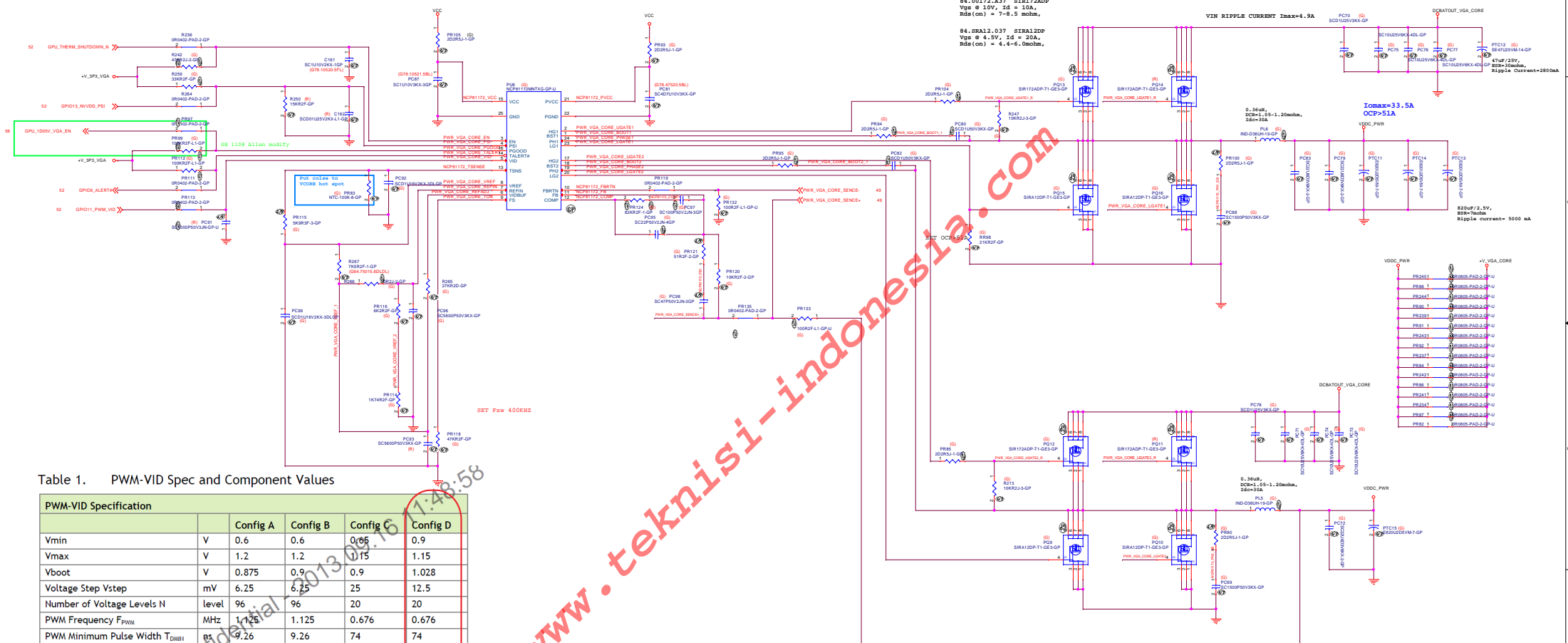


Table 1. PWM-VID Spec and Component Values

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F _{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T _{DMH}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

0.9V(NCP81172)
 $L=0.36\mu H$
 $\Delta I = (V_{in} - V_{out}) \cdot V_{out} / (V_{in} \cdot L \cdot F_{sw})$
 $\Delta I = ((19 - 0.9) \cdot 0.9) / (19 \cdot 0.36 \cdot 400K) = 5.95A$